出國報告（出國類別：國際會議）

出席 IEEE 2017 國際天線與傳播研討會及射頻無線電學術會議

服務機關：國立暨南國際大學 / 電機工程學系
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摘要

首先，感謝學校以及實驗室的補助和支持，學生才得以出席此年度的國際會議。此會議是國際電機電子工程師學會（Institute of Electrical and Electronics Engineers, IEEE）在 2017 年舉辦的國際天線與傳播研討會及射頻無線電學術會議（AP-S Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting），其提供了關於天線、傳播、電磁工程、無線電科學等等領域，一個交流最新研究訊息的國際論壇。

本次學生出席此國際會議，是為了在會議上進行三篇口頭論文發表，將實驗室的研究成果刊登上國際期刊；並於閒暇時間，聆聽會場其它之主題演講，學習各種新穎的專業知識、並參觀會場上，各個贊助廠商的擺攤演示，一來可以了解目前大公司內部的最新科技趨勢，二來也可以了解，如何將所學所知應用在業界中。

另外，在本次的會議中，讓我有機會認識來自世界各地，年齡又大為不同的各式各樣的優秀研究學者及學生，讓我能夠從他們身上學習一些談吐的氣質和研究的方法，並且，對我來說更重要的是，能夠學習大家富含個人特色的報告呈現方式，這些對我之後的學生生涯、甚至職場生涯都有著莫大的啟發。希望以後還能夠有機會參與其他各種的相關領域之國際學術研討會，也再次謝謝學校以及實驗室的補助和支持，學生才得以出席此年度的國際會議。

目次

一、出席此次國際會議之目的

國際電機電子工程師學會在 2017 年舉辦的國際天線與傳播研討會及射頻無線電學術會議（AP-S Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting），其提供了關於天線、傳播、電磁工程、無線電科學等等領域，一個交流最新研究訊息的國際論壇。本次會議在美國聖地牙哥（San Diego）的曼徹斯特君悅酒店（Manchester Grand Hyatt hotel）舉行，會議時程從七月九日至七月十四日止，總共六日的時間，其中每天從早上八點至下午五點，同個時段都會分別在不同會議室中，舉行大量的演講，同時也有開辦相關的短期課程可以參與（為期一天）。並且會議同時也邀請了許許多多的廠商來現場作擺攤，同時也會有展覽的場次可以進去參觀。同時，此會議從 1963 年開始，每年度都會邀請全球相關領域的專家學者來共襄盛舉，隨著時間的推移，逐漸成為此領域中最大的研討會。

本次學生出席此國際會議，是為了在會議上進行三篇口頭論文發表，將實驗室的研究成果刊登上國際期刊；並於閒暇時間，聆聽會場其它之主題演講，學習各種新穎的專業知識、並參觀會場上，各個贊助廠商的擺攤演示，一來可以了解目前大公司內部的最新科技趨勢，二來也可以了解，如何將所學所知應用在業界中。

另外，在本次的會議中，讓我有機會認識來自世界各地，年齡又大為不同的各式各樣的優秀研究學者及學生，讓我能夠從他們身上學習一些談吐的氣質和研究的方法，並且，對我來說更重要的是，能夠學習大家富含個人特色的報告呈現方式，這些對我之後的學生生涯、甚至職場生涯都有著莫大的啟發。

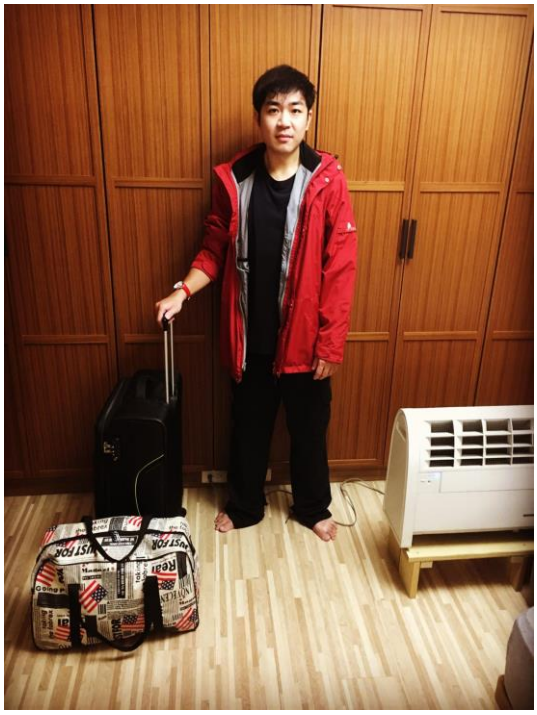
二、出國行程與會議經過

學生搭乘日航的班機，七月六日從高雄小港機場出發，抵達東京成田機場後轉機，並於當地時間七月六日中午抵達聖地牙哥國際機場，隨後搭乘當地的巴士前往 ITH Adventure Hostel San Diego 青年旅舍辦理入住。接著的七日、八日，學生則在當地探索城市、熟悉並認識周圍環境、順便習慣外語的環境、並且準備及複習報告所需資料及文件等等；同時也在青年旅舍認識了其他的與會成員。

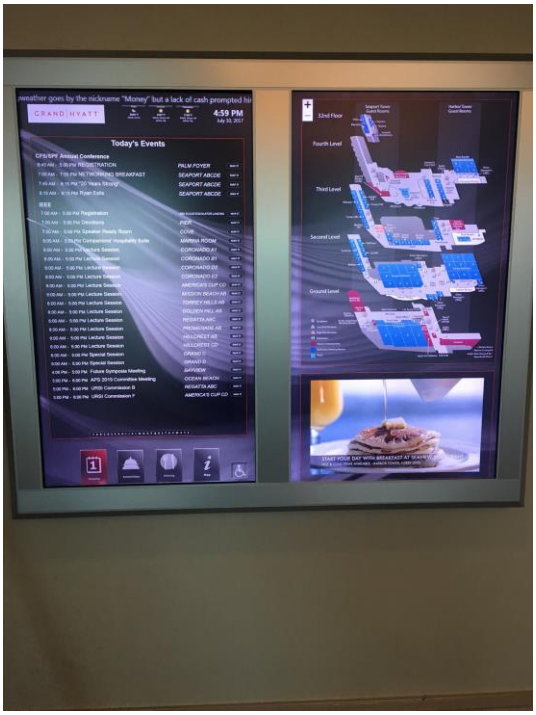
九日上午，學生徒步前往會議舉辦地點（曼徹斯特君悅酒店），並向三樓接待處辦理報到，取得會議相關資料及名牌，接著學生在會議舉辦地點進行場勘，確認口頭報告之場次及同地點之設備、並查看其它想聆聽之主題演講的舉辦時間和地點。

十日上午，學生徒步前往會議舉辦地點，並在早上九點至十一點，參與三樓 Torrey Hills AB 會議廳中，一場關於創新應用與檢測估計之方法的主題演講；並在中途的休息時間，享用大會提供的麵包、咖啡、牛奶、水果、餅乾等等，補充熱量和水分；並於十一點過後，聆聽於一樓大會場 Grand Hall C 舉辦的天線與射頻系統中額外製程製造之主題演講。十日下午，學生午餐過後，於下午一點至五點，參與三樓 Torrey Hills AB 會議廳中，一場關於射頻識別和量測系統之主題演講，以及另一場關於電磁模擬之教育教學和模擬工具軟體之主題演講，並在中途的休息時間，享用大會提供的點心，補充熱量和水分，以此為十日的行程畫下句點。

[2017 IEEE AP-S Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting website: http://2017apsursi.org/default.asp]

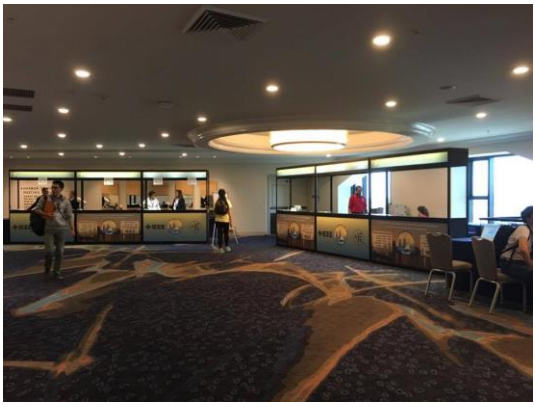


附圖一：準備出國前。



附圖二：當地會議地點地圖。

附圖三：會議地點。



附圖四：會議接待處。

附圖五：會議地點場勘。

十一日上午，學生徒步前往會議舉辦地點，並先進入準備室，確認口頭報告之投影片是否可正常啟動，並審視是否有須修改之錯誤，確認無誤後，學生在準備室順稿至午餐時間；並在午餐時，適當得調適緊張的心情。

十一日下午一點，學生即進入演講廳，等待口頭發表的時間到來；並聆聽當時的演講，主題則為指向性天線的寬頻饋入；十一日下午三點，待台上的演講結束之後，主持人指示可將投影片檔案匯入議場電腦，並測試運作是否正常，檢查投影機的投影即布幕，並請學生等待發表的時間到來。

十一日下午三點四十至四點，學生上台發表「95/190 GHZ PUSH-PUSH VCO IN 90 NM CMOS」；十一日下午四點至四點二十，學生上台發表「94 GHZ VCO USING NEGATIVE CAPACITANCE TECHNIQUE」；十一日下午四點四十至五點，學生上台發表「94 GHZ CMOS DOWN-CONVERSION MICROMIXER」。

不過因為學生此次出國為單獨行動，所以沒有人可以幫學生掌鏡、記錄上台發表的時刻，拜託聽講的觀眾掌鏡，又好像有點不合適；所以學生在發表結束之後，請會議主持人幫忙記錄學生發表的投影片，如下附檔六、附檔七、附檔八。

附檔六：學生上台發表「95/190 GHZ PUSH-PUSH VCO IN 90 NM CMOS」。

附檔七：學生上台發表「94 GHZ VCO USING NEGATIVE CAPACITANCE TECHNIQUE」。

附檔八：學生上台發表「94 GHZ CMOS DOWN-CONVERSION MICROMIXER」。

接著三天，十二日、十三日、十四日，學生都前往會場，並參與各種展覽，其中有包含其他與會成員的海報展覽、各大廠商的互動式展覽、或是享用會議地點提供的各種小點心，體驗一下異國風情、甚至也有書商的展場等等，如以下的附檔紀錄。

附檔九：展覽地點入口處。

附檔十：廠商展覽。

附檔十一：與會成員的海報展覽。

附檔十二：異國風味小點心。

附檔十三：廠商的互動式展覽。

三、個人心得與建議

此次為學生第二次出國參與國際會議，並且是學生首度進行口頭的論文發表，更是連續三場的演講演說，對學生無疑是個重大的挑戰；其中考驗了學生外語口說的邏輯組織力、口齒清晰與否、和對所發表論文之熟悉度與記憶力、並且還要準備各種聽講者可能提出的問題等等、更要適應來自世界各國的不同口音之外語等等；而學生為了保持演說的品質，所以選擇了進行大量的準備和練習，並嘗試克服眼前的難關；而最後的結果，學生覺得尚有缺點，其中最主要的是，在台上演說所造成的緊張感，是目前最大的阻礙，以及學生口說的語氣較為缺乏情緒等等，是學生自認尚須改進的缺點。

另外，學生在會場發現與會者們所發表之論文，有些已經可以應用在現實生活中，達成人類科技的進展，這是學生覺得極為佩服的，也是目前實驗室還在努力的方向。

這次出國所學到的寶貴經驗，學生會虛心學習、受教，並將之轉化為在學術生涯、或是未來職場生涯上的動力，期望未來的某一天，學生能夠有那麼一些些，接近世界上的同領域之頂尖研究者們。

最後，學生再次感謝學校以及實驗室的補助和支持，學生才得以出席此年度的國際會議，並得到審視自身不足的缺點的機會，希望未來學生還有機會能夠獲得補助，並參與其他盛大的國際會議。

四、附錄

發表論文。

95/190 GHz Push-Push VCO in 90 nm CMOS

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***Abstract*—A 95/190 GHz voltage-controlled oscillator (VCO) using gain-enhanced frequency doubler is demonstrated in 90 nm CMOS. Compared with the traditional push-push architecture, the proposed one can significantly increase the second-harmonic output signal due to the inductive series-peaking gain-enhancement of the full-wave-rectifier-based frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the transistors of the VCO. The VCO consumes 12 mW. At the fundamental port, the VCO achieves a tuning range of 92.6~95 GHz, and a low phase-noise of –88.2 dBc/Hz at 1 MHz offset from the center frequency. The corresponding FOM is –177 dBc/Hz. At the push-push port, the VCO achieves a tuning range of 185.2~190 GHz, and a low phase-noise of –82.5 dBc/Hz at 1 MHz offset from the center frequency. The corresponding FOM is –177.3 dBc/Hz. To the authors' knowledge, the phase noise and FOM performances of the VCO are one of the best results ever reported for a W-band or G-band CMOS VCO.**

***Keywords*—CMOS; push-push; VCO; W-band; G-bands**

I. Introduction

Normally, the fundamental oscillation frequency of an LC VCO is limited by the unity power gain frequency f_{max} of the cross-coupled transistors. To implement a VCO with oscillation frequency higher than f_{max}, push-push VCO, which uses the second-harmonic frequency tone based on nonlinearity of the cross-coupled transistors, has been proposed in [1]. However, the nonlinearity-based push-push VCO suffers from two issues. One is high power dissipation because high bias current is normally needed to generate sufficient second-order nonlinearity of the transistors. The other is that it is usually required to drive a high-impedance following stage, which makes it hard to be compactly implemented. In [2], a fundamental-signal-based push-push VCO using g_m-boosted full-wave rectification technique is proposed to enhance the second-harmonic output signal. Compared with the traditional full-wave rectification technique, the improvement in the second-harmonic output signal is smaller than 100%. In the present work, in order to achieve low power, low phase-noise, high output power (much higher than 100%), and high-frequency operation at the same time, we propose a 95/190 GHz push-push VCO using both the gain-enhancement frequency doubler and current reuse techniques. The second-harmonic output signal can be significantly enhanced due to the inductive series-peaking gain-enhancement of frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the cross-coupled transistors of the VCO.

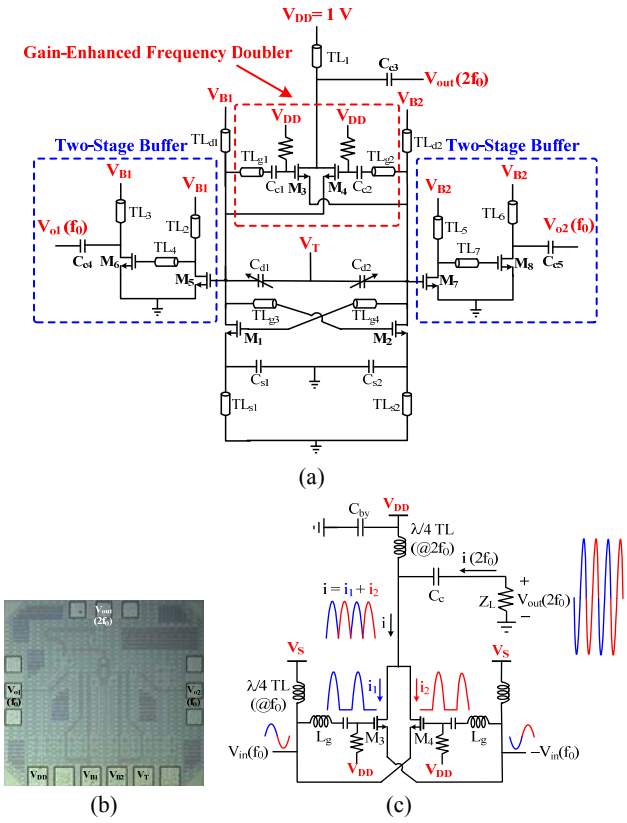

Fig. 1 (a) Circuit diagram, and (b) chip photo of the 95/190 GHz CMOS VCO. (c) The proposed frequency doubler.

II. Circuit Design

The push-push VCO with a full-wave-rectifier-based frequency doubler was designed by a 90 nm CMOS process. Fig. 1(a) shows the schematic of the proposed push-push VCO. Compared with the traditional push-push architecture, the proposed one can significantly increase the second-harmonic output signal due to the inductive series-peaking gain-enhancement of the frequency doubler. In addition, low power dissipation is achieved because the bias current of the frequency doubler is reused by the cross-coupled transistors of the VCO. Fig. 1(b) shows the chip micrograph of the push-push VCO. The chip area is only 0.58×0.61 mm^2, i.e. 0.35 mm^2, excluding the test pads. Fig. 2 illustrates the operation principle of the frequency doubler using the inductive series-peaking gain-enhancement technique. Transistors M_3/M_4 are biased at class-B, so each one contributes half-wave current rectification to realize the full-wave current rectification.

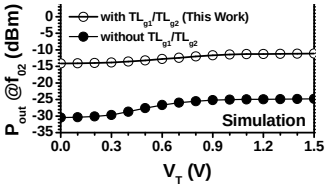

Fig. 3 Simulated single-ended output power at f_{02} versus V_T characteristics of the VCO

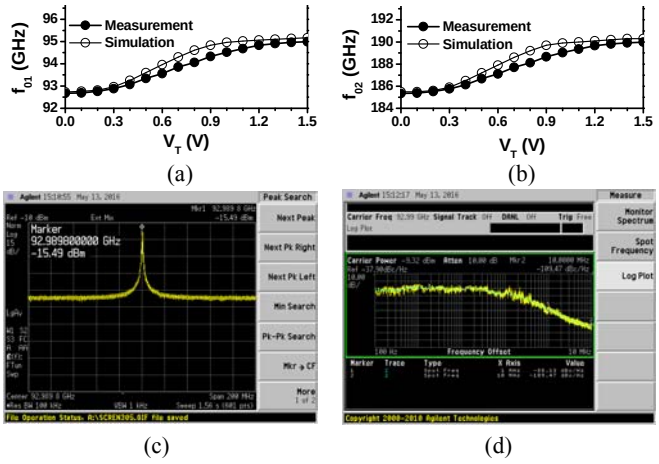

Fig. 4 Measured and simulated (a) f_{01} and (b) f_{02}, and measured (c) single-ended output spectrum, and (d) phase noise at f_{01} of the VCO.

Fig. 3 shows the simulated single-ended output power versus tuning voltage (V_T) characteristics at the push-push port of the VCO both with and without the series-peaking gain-enhanced inductors TL_{g1}/TL_{g2}. The VCO in our case achieves the better single-ended output power of –11.2~ –14.1 dB at the push-push port. In comparison, in the case without the peaking inductors TL_{g1}/TL_{g2}, the single-ended output power is only –24.8~ –30.4 dBm at the push-push port.

III. Circuit Design

The VCO core and buffer amplifiers draw bias currents from 1 V and 0.5 V power supply (Agilent 6624A), respectively. The VCO only consumes 12 mW. Fig. 4(a) shows the measured and simulated oscillation frequency versus V_T characteristics at the fundamental port of the VCO. The VCO achieves a tuning range of 92.6~95 GHz, close to that of the simulated one (92.7~95.2 GHz). Fig. 4(b) shows the measured and simulated second-harmonic frequency f_{02} versus V_T characteristics of the VCO. The VCO achieves a tuning range of 185.2~190 GHz, close to that of the simulated one (185.4~ 190.4 GHz). Fig. 4(c) shows the measured oscillation frequency and single-ended output power of the VCO at the fundamental port (at V_T = 0.35 V). The measured oscillation frequency is 93 GHz, and the corresponding single-ended output power (i.e., $V_{o1}(f_0)$ or $V_{o2}(f_0)$ only, the other port connected to a 50 Ω terminal) is –8.5 dBm (if the measured cable loss of 7 dBm is taken into account). Fig. 4(d) shows the measured phase noise of the VCO at the fundamental port at V_T = 0.35 V. The VCO achieves an excellent low phase-noise of –88.1 dBc/Hz at 1 MHz offset (from the center frequency of 93 GHz).

Table I Summary of the implemented 95/190 GHz CMOS VCO, and recently reported state-of-the-art MMW CMOS VCOs.

	P_{DC} (mW)	Freq. (GHz)	PN @1 MHz Offset (dBc/Hz)	FOM (dBc/Hz)	Process (nm)
This Work	12	95	88.2	177	90
		190	82.5	177.3	
[2]	14.6	80.7	84.2	166.9	90
[3]	54	105	92.8	175.9	65
[4]	15	97.2	80	168	90
[5]	2.6	70	78.7	171.5	110
[6]	10.4	59.3	81.7	167	65

A widely-used figure-of-merit (FOM) for a VCO is defined as follows.

$$\mathrm{FOM} = \mathrm{L}(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\ \mathrm{mW}}\right) \quad (1)$$

where $L(\Delta f)$ is the measured phase noise at Δf frequency offset from the carrier frequency f_o in dBc/Hz, and P_{DC} is the dc power dissipation in mW. Table I is a summary of the implemented 95/190 GHz CMOS VCO, and recently reported state-of-the-art millimeter-wave VCO. Compared with the measured results in other pieces of work, our VCO exhibits low power consumption and phase noise, and one of the best FOMs. These results indicate that our proposed VCO architecture is suitable for both W-band and G-band transceiver front-end applications.

IV. Conclusion

In this work, we propose a push-push VCO with a full-wave-rectifier-based frequency doubler, in which the inductive series-peaking gain-enhancement technique is used to improve the second-harmonic output signal. Since the bias current of the frequency doubler is reused by the VCO core, low power dissipation is available. At both the fundamental and push-push ports, the VCO achieves excellent tuning range, phase noise and FOM performances, one of the best results ever reported for a W-band or G-band VCO. These excellent results lead to the conclusion that the proposed VCO is suitable for both W-band and G-band communication systems.

References

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94 GHz VCO Using Negative Capacitance Technique

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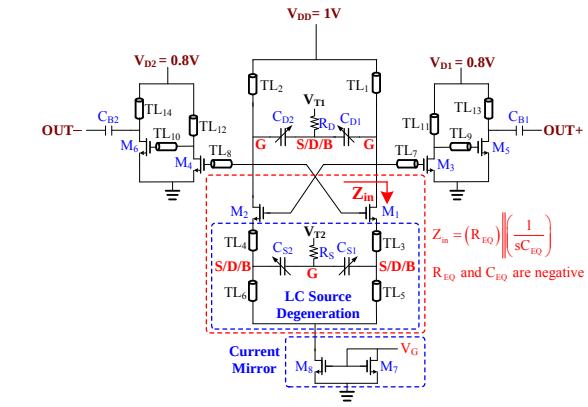
***Abstract*—A 94 GHz voltage-controlled oscillator (VCO) using both LC-source-degeneration-based (LCSD-based) negative capacitance technique and series-peaking gain enhancement technique is demonstrated in a 90 nm CMOS process. The LCSD-based negative capacitance is made by adding two tunable LC tanks, which use NMOSFET varactors as the needed capacitors, to the source terminals of the cross-coupled transistor pair of the VCO. Compared with the traditional cross-coupled transistor pair, the proposed one significantly decreases the tunable equivalent parallel capacitance (C_{EQ}) to zero and even a negative value. This in turn results in the increase of both the operation frequency and the tuning range of the VCO. The VCO draws 8.3 mA current from a 1 V power supply, i.e. it only consumes 8.3 mW. The VCO achieves a tuning range of 91~96 GHz. In addition, the VCO achieves an excellent low phase-noise of −98.3 dBc/Hz at 1 MHz offset from 95.16 GHz. The corresponding FOM is −188.5 dBc/Hz, one of the best results ever reported for a V- or W-band CMOS VCO. The circuit occupies a small chip area of 0.75×0.42 mm^2, i.e. 0.315 mm^2, excluding the test pads.**

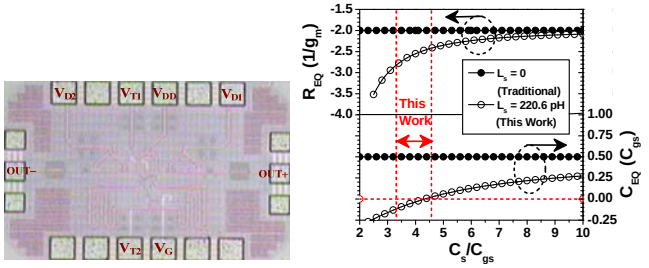
Keywords—CMOS; VCO; negative capacitance; W-band

I. Introduction

Some of the negative-resistance-cell-based oscillator architectures include ring oscillator, relaxation oscillator, and LC oscillator. Nowadays, in high-speed transceiver applications, LC VCO is the most popular one mainly because high-Q integrated inductors are available. The traditional negative-resistance cell constitutes a crossed-coupled transistor pair. The corresponding input impedance is equal to a negative resistance of $-2/g_m$ in parallel with a capacitance of $C_{gs}/2$, where g_m and C_{gs} are the transconductance and the gate-source capacitance of transistor, respectively [1]. For high frequency LC VCO, the ratio of $C_{gs}/2$ to the equivalent capacitance of the LC tank is high, which in turn degrades the operation-frequency and the tuning-range. Recently, researchers have made some proposals to reduce the parasitic capacitance of the traditional negative-resistance cell. For instance, the capacitive source-degeneration negative-resistance cell is proposed in [2]; however, only simulation data are available and the operation-frequency of 5.3 GHz is not high enough. In [3]-[4], the LC source-degeneration negative-resistance cell is proposed to further reduce the power dissipation, and the push-push technique is used to achieve dual-band operation. In this work, we propose a 94 GHz VCO using both the LCSD-based negative capacitance and the series-peaking gain enhancement techniques. The tunable equivalent parallel capacitance (C_{EQ}) of the cross-coupled transistor pair can be reduced to zero and even a negative value. This is the way to enhance the operation frequency and the tuning range of the VCO.



(a)



(b) (b)

Fig. 1 (a) Schematic diagram, and (b) chip micrograph of the proposed 94 GHz VCO. (c) Calculated R_{EQ} and C_{EQ} versus C_s/C_{gs} characteristics in the condition of $\omega/\omega_T = 0.549$ based on (3)-(4).

II. Circuit Design

Fig. 1(a) shows the schematic of the proposed VCO. The current mirror constitutes transistors M_7 and M_8 can provide stable bias current to the VCO core. Fig. 1(b) shows the chip micrograph of the proposed VCO. The chip area is only 0.75×0.42 mm^2, i.e. 0.315 mm^2, excluding the test pads. The equivalent L_s and C_s of the proposed LCSD-based cross-coupled transistor pair can be expressed as follows.

$$L_s \approx TL_3 + TL_5 \tag{1}$$

$$C_s \approx \frac{C_{s1}}{1+TL_3/TL_5} \tag{2}$$

After calculation, equivalent resistance R_{EQ} and equivalent capacitance C_{EQ} can be derived as follows:

$$R_{EQ} = \frac{-2}{g_m} \cdot \frac{[1+(\frac{\omega}{\omega_T})^2(1+\frac{C_s}{C_{gs}})^2 - 2(\frac{\omega_1}{\omega_T})^2(1+\frac{C_s}{C_{gs}})] + \frac{\omega_1^4}{\omega^2\omega_T^2}}{[(\frac{\omega}{\omega_T})^2\frac{C_s}{C_{gs}}(2+\frac{C_s}{C_{gs}}) - 2(\frac{\omega_1}{\omega_T})^2(1+\frac{C_s}{C_{gs}})] + \frac{\omega_1^4}{\omega^2\omega_T^2}}$$

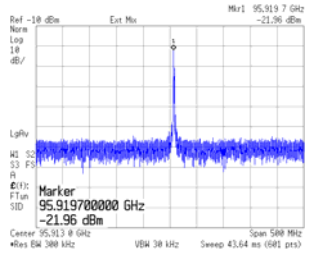
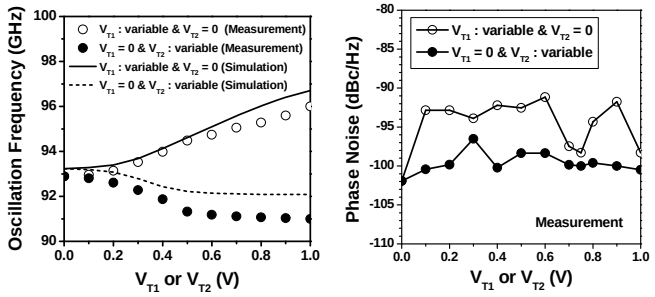


Fig. 2 Measured single-ended output spectrum.



(a) (b)

Fig. 3 (a) Measured and simulated oscillation frequency, and (b) measured phase noise versus V_{T1} or V_{T2} characteristics of the VCO.

Table I A summary of the 94 GHz CMOS VCO, and recently reported state-of-the art VCOs with similar operation frequency.

	V_{DD} (V)	P_{DC} (mW)	ω_0 (GHz)	PN (dBc/Hz)	FOM (dBc/Hz)	CMOS Process (nm)
This Work	1	8.3	93.6	–98.3	–188.5	90
[1]	1.2	54	105	–92.8	–175.9	65
[2]	1.2	15	97.2	–80	–168	90
[3]	1.2	2.6	70	–78.7	–171.5	110
[4]	1	10.4	59.3	–81.7	–167	65

$$\approx \frac{-2}{g_m} \quad (\text{if } C_s \text{ and } L_s \to 0) \tag{3}$$

$$C_{EQ} = \frac{C_s}{2} \cdot \frac{\frac{\omega_2^2}{\omega^2} + \frac{\omega_1^2}{\omega_T^2}\frac{\omega_2^2}{\omega^2} + \frac{\omega^2}{\omega_T^2}\left(1+\frac{C_s}{C_{gs}}\right) - \frac{\omega_1^2}{\omega_T^2} - \frac{\omega_2^2}{\omega_T^2}\left(1+\frac{C_s}{C_{gs}}\right) - 1}{\frac{\omega_1^4}{\omega^2\omega_T^2} + \frac{\omega^2}{\omega_T^2}\left(1+\frac{C_s}{C_{gs}}\right)^2 - 2\frac{\omega_1^2}{\omega_T^2}\left(1+\frac{C_s}{C_{gs}}\right) + 1}$$

$$\approx \frac{C_{gs}}{2} \quad (\text{if } C_s \text{ and } L_s \to 0) \tag{4}$$

in which $\omega_T = g_m/C_{gs}$ is the current-gain cut-off frequency of the cross-coupled transistors M_1 and M_2, $\omega_1 = 1/\sqrt{L_s C_{gs}}$, and $\omega_2 = 1/\sqrt{L_s C_s}$.

Fig. 1(c) shows the calculated R_{EQ} and C_{EQ} versus C_s/C_{gs} characteristics in the condition of $f/f_t = 0.549$. As can be seen, C_{EQ} decreases with the decrease of C_s/C_{gs}. The expense is an increase of the magnitude of the negative resistance R_{EQ}. That is, there is a trade-off between C_{EQ} reduction and the possibility of oscillation start-up. To minimize C_{EQ} for high frequency operation and to make sure oscillation start-up, selection of a C_s/C_{gs} value below than 8 is reasonable. In this work, corresponding to V_{T2} tuning range of 0~1 V, C_s/C_{gs} ranges 3.3~4.6. The corresponding R_{EQ} and C_{EQ} are $-2.41/g_m$ ~ $-2.83/g_m$ and 0 ~ $-0.118C_{gs}$, respectively. Since C_{EQ} is equal to zero or a negative capacitance (for reducing the overall capacitance of the VCO), both the operation frequency and the tuning range of the VCO can be effectively enhanced.

III. Results and Discussions

The VCO core and buffer amplifiers draw bias currents from 1 V and 0.8 V power supplies, respectively. The VCO only consumes 8.3 mW. Fig. 2 shows the measured oscillation frequency and single-ended output power of the VCO at V_{T1} = 1 V and V_{T2} =0 V. The measured oscillation frequency is 95.92 GHz, and the corresponding single-ended output power (i.e., OUT+ or OUT– only, the other port connected to 50 Ω terminal) is –14 dBm (if the measured cable loss of 8 dBm is considered).

Fig. 3(a) shows the measured and simulated oscillation frequency versus V_{T1} or V_{T2} characteristics of the VCO. The VCO achieves a tuning range of 91~96 GHz, close to that of the simulated one (92.1~96.7 GHz). In addition, the VCO achieves single-ended output power of –8.2~ –14.1 dBm (not shown here). Fig. 3(b) shows the measured phase noise (at 1 MHz offset from the center frequency) versus V_{T1} or V_{T2} characteristics of the VCO. The VCO achieves phase noise of –91.2~ –101.9 dBc/Hz. Table I is a summary of the implemented 94 GHz CMOS VCO, and recently reported state-of-the-art VCO with similar operation frequency. Compared with the measured results in other pieces of work, our VCO exhibits low power consumption, and one of the best phase noises and FOMs. These results indicate that our proposed VCO architecture is suitable for both V- and W-band transceiver front-end applications.

IV. Conclusion

In this work, we propose a CMOS VCO architecture using LCSD-based negative capacitance technique and the series-peaking gain enhancement technique. The VCO achieves a tuning range of 91~96 GHz, and a low phase-noise of –98.3 dBc/Hz at 1-MHz offset from 95.16 GHz. The corresponding FOM is –188.5 dBc/Hz, one of the best results ever reported for a W-band CMOS VCO. These results indicate that the VCO is suitable for V- and W-band communication systems.

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94 GHz CMOS Down-Conversion Micromixer

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***Abstract*—A W-band (75~110 GHz) down-conversion mixer for 94 GHz image radar sensors in 90 nm CMOS is reported. Micromixer-based gain-enhanced technique, i.e. inductive series-peaking gain-enhanced single-in differential-out (SIDO) class-AB RF GM stage, is used to increase the output impedance and suppress the feedback capacitance C_{gd} of RF GM stage. Hence, conversion gain (CG), noise figure (NF) and LO-RF isolation of the mixer can be enhanced. The mixer consumes 7.2 mW and achieves excellent RF-port input reflection coefficient of –10~–14.4 dB for frequencies of 81.4~110 GHz. The corresponding –10 dB input matching bandwidth is greater than 28.6 GHz. In addition, for frequencies of 90~96 GHz, the mixer achieves CG of 10.5~12 dB (the corresponding 3-dB CG bandwidth is 22 GHz) and LO-RF isolation of 40.2~46.2 dB, one of the best CG and LO-RF isolation results ever reported for a down-conversion mixer with operation frequency around 94 GHz. Furthermore, the mixer achieves an input third-order intercept point (IIP3) of 1 dBm at 94 GHz. These results demonstrate the proposed down-conversion mixer architecture is very promising for 94 GHz image radar sensors.**

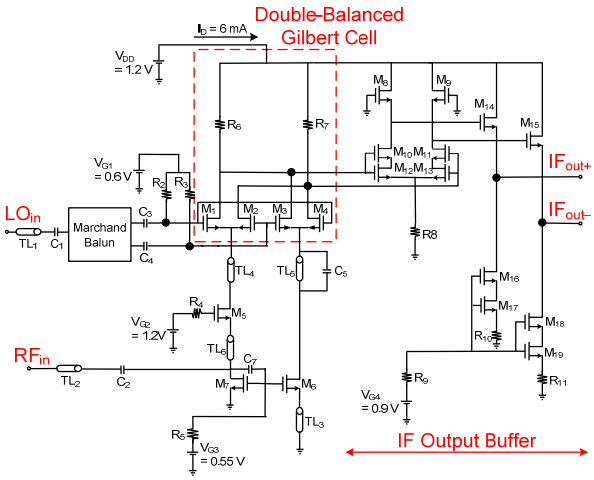
Keywords—CMOS; 94 GHz; down-conversion micromixer

I. INTRODUCTION

Thanks to the rapid development of CMOS processes, it has become possible to use them to implement W-band RFICs [1]-[3]. In transceiver design, down-conversion mixer is a critical block that receives signals from LNA over the band of interest, and then amplifies and down-converts the signals with a good SNDR property. In addition to low power, the basic requirements for a down-conversion mixer include good input and output impedance matching, high port-to-port isolation, low NF, and high CG over the band of interest. Nowadays, researchers have introduced several splendid W-band CMOS and GaAs mixers for down-conversion [1]-[3]. For instance, in [1], a 77 GHz double-balanced mixer for down-conversion in 65 nm bulk CMOS technology (with f_T higher than 150 GHz) is reported. The mixer has two transformer-based baluns that convert RF and LO inputs to differential outputs. Excellent power performance of 6 mW is obtained. However, CG of –8 dB and LO-RF isolation of 21 dB are unsatisfactory. In [2], a 94 GHz down-conversion mixer using branch line couplers in 0.1 μm GaAs process (with f_T of 189 GHz) is demonstrated. Similarly, its performances such as CG of –14.7 dB, LO-RF isolation of 35.2 dB and chip area of 3.38 mm^2 are not good enough. In this work, we report a 94 GHz down-conversion micromixer in 90 nm CMOS (with f_T of 130 GHz).

II. CIRCUIT DESIGN

The 94 GHz down-conversion micromixer was designed and implemented in 90 nm CMOS. Fig. 1(a) illustrates the circuit diagram of the double-balanced mixer for direct down-conversion. The mixer is made up of a double-balanced Gilbert cell with an inductive series-peaking gain-enhanced single-in differential-out (SIDO) class-AB RF GM stage, one miniature planar Marchand balun that converts LO input to



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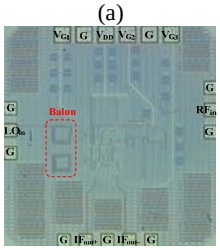
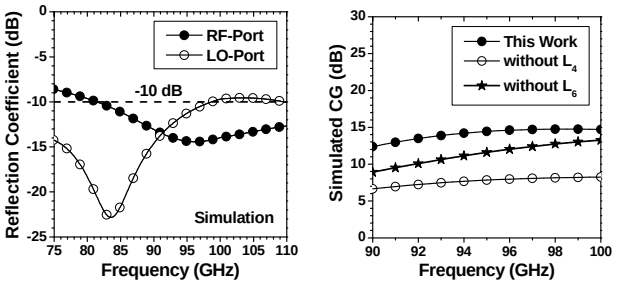


(b)

Fig. 1 (a) Schematic diagram, and (b) chip microphotograph of the 94 GHz CMOS down-conversion micromixer.

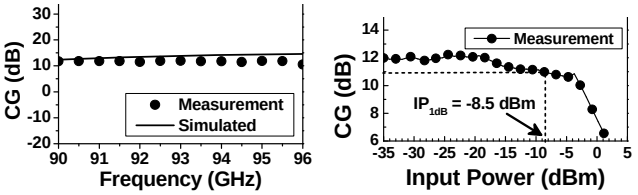


(a) (b)

Fig. 2 Simulated (a) RF-port and LO-port reflection coefficients, and (b) CG versus frequency characteristics of the micromixer

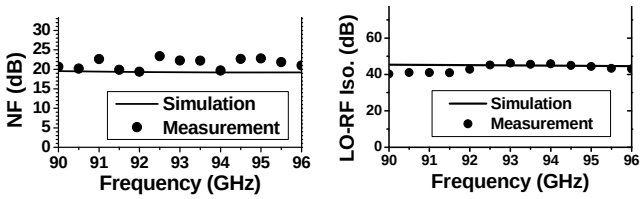
Table I Summary of the implemented DC micromixer, and recently reported state-of-the-art W-band DC mixers.

Reference	Process	Topology	RF Frequency (GHz)	LO Power (dBm)	CG (dB)	LO-RF Isolation (dB)	NF (dB)	Power (mW)	FOM (no unit)
This Work	90-nm CMOS	Micromixer-based Gain-Enhanced RF GM Stage	94	0	11.7	45.8	19.7	7.2	4.37×10^{-4}
[1] (2009 MWCL)	65-nm CMOS	Gilbert-Cell with On-Chip Baluns	76~77	4	–8	21	17.8	6	1.01×10^{-4}
[2] (2012 GSMM)	100-nm GaAs	Single-Balanced Using Branch Line Couplers	94	10	–14.7	35.2	NA	NA	NA
[3] (2008 MWCL)	90-nm CMOS	Sub-harmonic Gilbert-Cell	30~100	10	–1.5	47	NA	58	NA



(a) (b)

Fig. 3 (a) Measured and simulated CG versus frequency, and (b) measured CG versus RF power characteristics of the micromixer.



(a) (b)

Fig. 4 Measured and simulated (a) NF, and (b) LO-RF isolation versus frequency characteristics of the micromixer.

differential output, and an IF output buffer. Fig. 1(b) shows the chip micrograph of the down-conversion micromixer. The chip area is 0.88×0.74 mm^2 (i.e. 0.651 mm^2).

Fig. 2(a) shows the simulated input reflection coefficients at RF-port (S_{11}) versus frequency characteristics of the down-conversion micromixer. The micromixer achieves S_{11} of −14.2 dB at 94 GHz, minimal S_{11} of −14.4 dB at 96.2 GHz, and S_{11} smaller than −10 dB for RF frequencies of 81.4~110 GHz. What is also shown in Fig. 2(a) is the simulated input reflection coefficients at LO-port (S_{22}) versus frequency characteristics of the down-conversion mixer. The mixer achieves S_{22} of −11.7 dB at 94 GHz, minimal S_{22} of −22.8 dB at 83.6 GHz, and S_{22} smaller than −10 dB for LO frequencies of 61.3~98.7 GHz.

Fig. 2(b) shows the simulated CG versus frequency characteristics of the micromixer in various conditions. RF input power is −35 dBm and LO input power is 0 dBm. For the case with both the series-peaking inductors L_4 and L_6 (i.e. this work), the micromixer achieves CG of 12.4~14.8 dB for frequencies of 90~100 GHz, better than that (CG of 6.7~8.2 dB for frequencies of 90~100 GHz) for the case without L_4, and that (CG of −8.9~13.3 dB for frequencies of 90~100 GHz) for the case without L_6.

III. Results and Discussions

Fig. 3(a) shows the measured and simulated CG versus frequency characteristics of the micromixer. RF input power is −35 dBm and LO input power is 0 dBm. For frequencies of 90~96 GHz, the mixer achieves CG of 10.5~12 dB, close to that (12.4~14.6 dB) of the simulated one. In addition, the 3dB CG bandwidth of the mixer is 22 GHz (not shown here). Fig. 3(b) shows the measured CG versus RF input power characteristics of the mixer. The mixer achieves an excellent input P_{1dB} of −8.5 dBm, and an IIP3 of 1 dBm (not shown here).

Fig. 4(a) shows the measured and simulated NF versus frequency characteristics of the mixer. The measured result conforms with the simulated one well. The mixer achieves minimal NF of 19.4 dB at 92 GHz, and NF of 19.4~22.7 dB for frequencies of 90~96 GHz. Fig. 4(b) shows the measured and simulated LO-RF isolation versus frequency characteristics. The measured result conforms with the simulated one well. The mixer achieves maximal LO-RF isolation of 46.2 dB at 93 GHz, and LO-RF isolation of 40.2~46.2 dB for frequencies of 90~96 GHz. The excellent LO-RF isolation is mainly attributed to the LO-RF leakage through capacitance C_{gd6} of the RF GM stage transistor M_6 is suppressed by TL_5/C_5. To the authors' knowledge, this is one of the best LO-RF isolation results ever reported for a W-band down-conversion mixer (see Table I).

IV. Conclusion

We demonstrate a 94 GHz CMOS down-conversion mixer. The mixer is made up of a double-balanced Gilbert-cell with an inductive series-peaking gain-enhanced SIDO class-AB RF GM stage, one LO-port balun, and an IF output buffer. The mixer dissipates 7.2 mW and obtains remarkable CG and LO-to-RF isolation performances. This result indicates that the mixer is promising in W-band systems.

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