出國報告（出國類別：其他-國際會議）

參加「二〇一六年IGBSG國際研討會」出國報告

服務機關：國立雲林科技大學電機系
姓名職稱：林伯仁教授
派赴國家：捷克/布拉格
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摘要

6 月 27~29 日參加二〇一六年 IGBSG 國際會議，出席會議之目的是向各國電機電子專家學者討論綠色智慧建築與智慧電網應用趨勢與介紹個人在此方面之研究成果，並向各國交流此方面之發展趨勢。學習各國學者與業界工程師在電力電子技術、能源技術與智慧電網應用發展。研討會期間與捷克專家學者互相討論電力電子技術與智慧電網等相關問題，以提升在電力電子方面的研究方向。筆者在研討會中發表數種應用於高壓直流電源轉換器之電路架構來達到高效率及低損耗之優點，有深入之討論與答辯，此幾種電路架構都具有高效率電路轉換之優點以節省能源損耗，最後利用硬體電路實現來證明所提新型高壓直流電源轉換器之實用性與優越性。參加此次 IGBSG 研討會獲得很多國外之研究成果，也同時詳細向國外學者介紹台灣之研究近況與績效。

目次

一、 目的

參加二〇一六年IGBSG國際研討會之主要目的為: 1.發表筆者近兩年在高效率電源轉換之研究成果，2.與各國專家學者討論最新之研究趨勢，3.與國際綠色能源專家學者廣泛討論智慧電網技術與科技趨勢，4.向國際學者介紹台灣在高效率綠色能源轉換器技術之研究成果。

二、 過程

二〇一六年IGBSG國際綠色智慧建築與智慧電網應用研討會在捷克/布拉格召開，會議時間自6月27日至6月29日。主辦單位為捷克科技大學，承辦單位為台灣科技大學。此研討會提供了一個給電機、電子學術界能相互交流的環境，並探討創新的思路與發展的新興領域及電力電子和信號處理，控制和系統等相關課題。IGBSG會議是每兩年舉辦一次的國際學術研討會，每兩年會議會在歐洲與亞洲各國家舉辦。此次在捷克舉辦之研討會投稿篇數為98篇，智慧建築之控制與感測文章有13%，通訊網路與應用文章有17%，綠色通訊網路文章有16%，綠色積體電路與系統文章有15%，能源系統發展文章有12%，智慧電力系統文章有27%。投稿全文經多位審稿者無記名審查，通過審查共有46篇論文於會議中發表，文章接受率約為47%。會議中安排有三場主題演講，會議內容共有9個時段之論文發表分別於6/27至6/29舉行。6/27日至6/29日參加各場次之論文發表會，筆者在2016年6月28日於布拉格當地時間早上十點半到十二點半，在捷克理工大學session 2B會議室進行兩篇論文報告:

1. Analysis of a New Resonant Converter with Auxiliary Windings to Extend Input Voltage Range
2. Implementation of a Modular Full-Bridge DC/DC Converter

筆者論文中發表兩種不同方法之高效率直流電源轉換器架構，此兩種電路對實現高效率及低損耗的電源供應器有深入討論，電路架構之優勢為具有零電壓切換技術，文章中利用硬體電路實現結果來證明所提新型電力轉換器之實用性與優越性能，此兩篇文章獲得捷克學者之興趣，有熱烈討論與互相交流。有捷克學者問到電路之優點與運用方面問題，筆者告訴此學者第一篇論文之電路架構可以增加消費性電源供應器在交流電源斷路時之保持時間，因為電路中二次側增加一組備用線圈，因此諧振電路具有高電感比，比傳統電路有較高電路效率及節省能源損耗。而筆者第二篇文章之電路架構可以用於捷運軌道車直流電源系統，因為軌道車之直流電壓高達 750V 因此筆者使用三階全橋相移電路，利用模組化及三階技術，來達到每個模組電路電流平衡與個別控制之要求，以便於故障之排除，為了達到輸入電容電壓平衡問題，飛輪平衡電容加入在輸入端以便達到次要求。對於筆者之詳細解說與答辯，捷克學者感到非常滿意並邀請有機會到捷克科技大學進行一次學者訪問或演講。個人在會議過程中參加了智慧電網、再生能源與高功率電源技術等各項論文發表場次

，會後也與各作者有近一步之互動與討論，大家也互相交換名片做為將來互相書信與郵件通信用。此會議為一有關綠色智慧建築與智慧電網應用之國際研討會，會議內容包含能源技術、智慧電網技術與再生能源應用。我國是能源進口國，依賴能源非常嚴重，因此如何節省能源與提高能源利用率是很重要，再生能源之發展可以部份解決此一問題，而如何利用電力電子技術來提高能源轉換之效率是筆者多年來一直努力研究之目標，筆者多年來參加再生能源轉換相關之國際研討會希望能對國內再生能源技術之提升能做出一些貢獻。

三、 心得

IGBSG 國際會議為有關電力電子技術、智慧電網及能源技術相關研究方面重要會議之一。本次會議共有 46 篇論文。台灣有很多師生參與，包括台灣科技大學、成功大學及其他國內私立大學教授等人員參加。為提高台灣之學術地位及能見度，仍需科技部與教育部繼續支持。在本次的會議中可以看出論文品質提升，在會議中能認識其他國家的人士，彼此能交換心得，對於開拓視野、提升研究品質有莫大的幫助。會中與各國專家學者交換意見，獲益良多。茲將出席本次會議心得分述如下：

1. 台灣學者在研究品質上與各國相比較，表現很好。
2. 與各國專家學者交換電源轉換器與智慧電網技術，獲益良多。
3. 與捷克學者在大會上廣泛互動與討論研究方向，作為將來合作之機會。
4. 此次會議中較多研究論文發表集中智慧電網能源轉換技術。
5. 雲端電源技術之發展，在此次研討會中也是被討論主題之一。

四、 建議事項

IGBSG 國際會議是有關綠色智慧建築與智慧電網相關研究方面的重要國際會議，主要是台灣與捷克兩國在多年前一起舉辦之國際會議，會議中所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對智慧電網之發展有提出多篇重要之研究方向，研討會過程中，發現國內的研究水平尚屬優良，研究內容亦受到眾多人的興趣，且整體的素質都受到肯定。大會提供給與會人員研討會相關之文章介紹。裡面包含 IGBSG 2016 國際綠色建築與智慧電網研討會所有論文集。由於參與類似的學術性會議非常重要，因此希望政府多鼓勵國內學者積極參與此類型之國際學術會議及加強補助此領域之研究。

五、 附錄

發表論文資料。

Implementation of a Modular Full-Bridge DC/DC Converter

B.R. Lin, *Senior Member, IEEE,* and Sheng-Zhi Zhang
Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin 640, Taiwan

***Abstract*–In this paper, the modular multilevel dc/dc converters, by integrating the full-bridge converters in series, are provided for high power and high voltage dc-based systems. Each circuit module includes a full-bridge converter and a half-bridge LLC resonant converter to implement the wide range of soft switching and low conduction losses. The ZVS condition of the power switches at the leading leg is implemented by the energy stored on the output inductor. The ZVS condition of power switches at the lagging leg is implemented by the LLC resonant converter. Therefore, all switches can be turned on at ZVS from light load. A passive snubber is adopted on the secondary side of full-bridge converter to reduce the conduction loss during the freewheeling interval especially at high input voltage and full load conditions. The outputs of the full-bridge converter and resonant converter are series connection. Therefore, energy is transferred by both converters at whole switching period. Two circuit modules are connected input-series and output-parallel to effectively limit the voltage rating of switches at $V_{in}/2$. Flying capacitor is adopted in the proposed circuit to balance input voltages in each switching cycle without the complexity control scheme. Finally, Experiments with a 1920W prototype are provided to demonstrate the performance of the proposed circuit.**

Keywords—full-bridge converters; zero-voltage switching, LLC.

I. Introduction

Multilevel converters for ac motor drivers [1], reactive power compensators [2], high voltage dc distribution systems [3] and dc-based data storage systems [4] have been proposed and studied for many years. The circuit topologies of multilevel converters are based on the series-connected full-bridge circuits, flying capacitor topologies or clamped diodes to reduce the voltage stress of power semiconductors. For multilevel dc/dc converters, soft switching three-level pulse-width modulation converters have presented in [5]-[7] to limit voltage stress of power semiconductors at $V_{in}/2$, decrease the switching losses and increase the circuit efficiency. The phase shift pulse-width modulation (PS-PWM) is adopted to generate the gate signals of power switches. The active switches at the leading leg can be easily turned on at zero voltage switching (ZVS) due to the energy stored on the output inductor is reflected to the primary side to discharge the output capacitance of switches. However, the first shortcoming of the PS-PWM scheme is the narrow ZVS load range of the switches at the lagging leg switches due to the limited energy stored on the primary leakage inductor. The other problem is the high conduction losses when the primary side is operated at freewheeling state. To extend the ZVS range, a large leakage inductance or an external resonant inductance [8] or half-bridge converter [9] can be used on the primary side. However, the large inductance will results in high duty cycle loss and low effective duty cycle. Therefore, the lower turns ratio transformer must be used. The lower turns ratio transformer will increase the primary conduction losses. To reduce the high circulating current losses, active components or passive components [10] are adopted at the output side to reduce voltage overshoots and oscillations across the output diodes. Therefore, the primary current can be reduced to zero when the converter is operated at freewheeling state.

A modular multilevel dc/dc converter is presented to achieve low conduction loss and wide ZVS range. The proposed circuit topology is input-series and output-parallel of two circuit modules with one flying capacitor. Thus, the voltage rating of power switches is reduced and low voltage rating switches can be used in the proposed converter. One flying capacitor connected between two circuit modules can be used to balance input capacitor voltages. In each circuit module, full-bridge converter with *LLC* converter sharing the lagging-leg switches can achieve the wide ZVS range of all switches. The passive snubbers are used on the secondary side to decrease the primary current to zero. Thus, the high conduction loss in conventional PS-PWM full-bridge circuit is improved. The output voltages of the *LLC* converter and the full-bridge converter are series connection. Thus, energy can be delivered by both converters during the entire switching period. Finally, experiments with a laboratory circuit rated at 1920W are provided to show the performance of the proposed circuit.

II. Circuit Diagram

Fig. 1 illustrates the circuit diagram of the modular three-level converter for high voltage dc-based applications such as dc-based distributions and dc-based data storage systems. The circuit topology is based on the input-series and output-parallel of two circuit modules with one flying capacitor connected between points a and d to autobalance input split capacitor voltages v_{Cin1} and v_{Cin2} at $V_{in}/2$. Each circuit module delivers one half of the rated power to the output load. The voltage rating of power switch is limited at $V_{in}/2$. Therefore, the low voltage rating switches can be used with the advantages of low turn-on resistance and low conduction losses. Fig. 2 gives the main PWM waveforms of the modular dc-dc converter. Switches S_{1x} and S_{2x} have the same time sequence, where x=1, 2, 3 and 4. The PS-PWM scheme is used to generate the necessary PWM waveforms of power switches S_{11}~S_{24}. If switches S_{11} and S_{21} are in the on state and S_{14} and S_{24} are both turned off as shown in Fig. 3(a), then the flying capacitor voltage v_{Cf} =v_{Cin1} with time duration $T_s/2$. In the same manner, the flying capacitor voltage v_{Cf}=v_{Cin2} if S_{11} and S_{21} are in the off state and S_{14} and S_{24} are

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turned on with the time duration $T_{sw}/2$ as shown in Fig. 3(b). Therefore, it can obtain that $v_{Cin1}=v_{Cin2}=v_{Cf}=V_{in}/2$ and no additional active component or the complex control loop is needed to balance the input spilt capacitor voltages. The advantages of the proposed modular multilevel dc/dc converter are low conduction losses due to low circulating current, wide ZVS range due to resonant converter connected to the lagging-leg switches, less output inductor current ripple and voltage auto-balance ability.

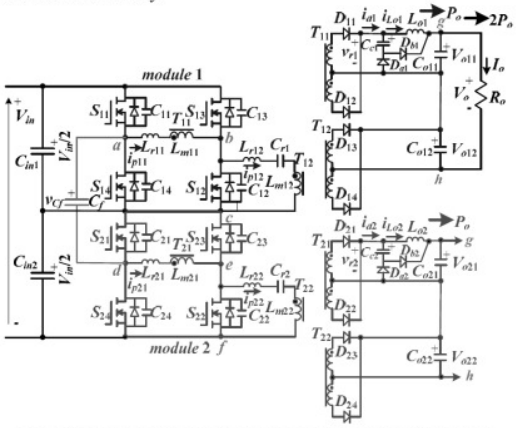


Fig. 1. Proposed modular multilevel dc/dc converter (a) circuit diagram.

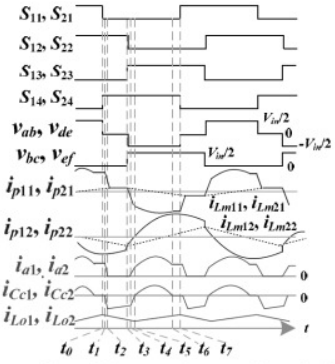


Fig. 2. key PWM waveforms of the proposed converter in a switching cycle.

The circuit module 1 includes a full-bridge converter (S_{11}-S_{14}, C_{11}-C_{14}, T_{11}, L_{r11}, D_{11}, D_{12}, L_{o1}, C_{c1}, D_{a1}, D_{b1} and C_{o11}) and a *LLC* converter (S_{12}, S_{13}, C_{12}, C_{13}, L_{r12}, C_{r1}, T_{12}, D_{13}, D_{14} and C_{o12}). (S_{11} and S_{14}) and (S_{12} and S_{13}) are in the leading-leg and lagging-leg, respectively. Half-bridge *LLC* converter is worked at the constant duty cycle and constant switching frequency. Therefore, the output voltage V_{o12} is un-regulated. The energy stored on the output inductor L_{o1} is used to achieve ZVS of the switches S_{11} and S_{14} at the leading leg. The half-bridge *LLC* converter based on the series resonant inductor L_{r12}, resonant capacitor C_{r1} and the magnetizing inductor L_{m12} is operated at the inductive load condition. Therefore, the primary fundamental current i_{p12} is lagging to the primary fundamental voltage v_{bc} and the ZVS of the lagging-leg switches S_{12} and S_{13} are easily achieved from light load. The passive snubber circuit including C_{c1}, D_{a1} and D_{b1} is adopted on the secondary side to reduce the primary current to zero at freewheeling state. When v_{ab}=0 (freewheeling state), the diode D_{a1} conducts and the rectified voltage $v_{r1}=v_{Cc1}$. The reflected voltage $n_{11}v_{r1}$ is applied to L_{r11} to decrease the primary current i_{p11} to zero value. The output inductor voltage $v_{Lo1}=v_{Cc1}-v_{o11}$ instead of $-v_{o11}$ in the conventional full-bridge converter so that the size of the output inductor L_{o1} is reduced. Since the output voltages of the full-bridge converter and the *LLC* converter are series connection, the resonant converter can transferred energy for the entire switching period. Similarly, module 2 has the same circuit characteristics as module 1.

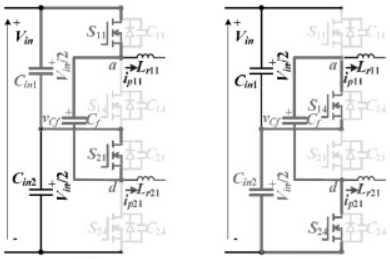


Fig. 3. Voltage autobalance scheme (a) $v_{Cf}=v_{Cin1}$ (S_{11} and S_{21} on) (b) $v_{Cf}=v_{Cin2}$ (S_{14} and S_{24} on)

III. Operation Principles

In the proposed modular multilevel converter, all components in each circuit module are identical $L_{r11}=L_{r21}$, $L_{r12}=L_{r22}$, $C_{r1}=C_{r2}$, $L_{o1}=L_{o2}$, $n_{11}=n_{21}$ and $n_{12}=n_{22}$. MOSFETs and rectifier diodes are assumed ideal. The voltages across C_{o11}~C_{o22} are constant. The output capacitances of switches C_{11}=….=C_{24}=C_{oss}. Based on the conduction states of power switches and rectifier diodes, there are seven topological stages in each half of switching cycle. Fig. 4 illustrates the equivalent circuits for each stage at the first half switching cycle.

***Stage 1* [t_0 - t_1]:** Prior to t_0, S_{11}, S_{12}, S_{21}, S_{22}, D_{11}, D_{14}, D_{21} and D_{24} conduct. The inductor currents $i_{p11}>0$, $i_{p12}<0$, $i_{p21}>0$ and $i_{p22}<0$. S_{11} and S_{21} are turned off at time t_0. i_{p11} (i_{p21}) charges C_{11} (C_{21}) and discharges C_{14} (C_{24}). The energy stored on L_{o1} (L_{o2}) is used to discharge C_{14} (C_{24}) to zero voltage. Therefore, the ZVS conditions of S_{14} and S_{24} are expressed in (1) and (2), respectively.

$$(L_{r11}+n_{11}^2L_{o1})i_{p11}^2(t_0)\geq 2C_{oss}(V_{in}/2)^2=C_{oss}V_{in}^2/2 \quad (1)$$

$$(L_{r21}+n_{21}^2L_{o2})i_{p21}^2(t_0)\geq C_{oss}V_{in}^2/2 \quad (2)$$

Since all components in circuit modules 1 and 2 are identical ($L_{r11}=L_{r21}$, $i_{p11}=i_{p21}$, $L_{o1}=L_{o2}$ and $n_{11}=n_{21}$), equation (1) and (2) can be further expressed as (3) if the current ripple on L_{o1} and L_{o2} can be neglected.

$$(L_{r11}/n_{11}^2+L_{o1})I_o^2\geq 2C_{oss}V_{in}^2 \quad (3)$$

Stage 1 ends at t_1 when v_{C14}=v_{C24}=0. The time duration at stage 1 is given in (4).

$$\Delta t_{01} = \frac{C_{oss} V_{in}}{i_{p1}(t_0)} \approx \frac{2n_1 C_{oss} V_{in}}{I_o} \quad (4)$$

The dead time between S_{11} (S_{21}) and S_{14} (S_{24}) must be greater than Δt_{01} to achieve ZVS of S_{14} and S_{24}.

***Stage 2* [t_1 - t_2]:** Capacitors C_{14} and C_{24} are discharged to zero voltage at time t_1. Therefore, v_{ab}=v_{de}=0 and diodes D_{a1} and D_{a2} conduct. The inductor voltages v_{Lo1}=v_{Cc1}-V_{o11}<0 and v_{Lo2}=v_{Cc2}-V_{o21}<0 so that i_{Lo1} and i_{Lo2} decrease. Since $i_{p11}(t_1)$ and $i_{p21}(t_1)$ are both positive, the anti-parallel diodes of S_{14} and S_{24} conduct. Therefore, the ZVS of S_{14} and S_{24} is achieved at t_1. The reflected secondary windings voltages -$n_{11}v_{Cc1}$ are applied to L_{r11} and L_{r21}, respectively and the primary currents i_{p11} and i_{p21} rapidly decrease to zero at time t_2. Thus, the conduction losses at freewheeling state are removed. The time interval in this stage is given as $\Delta t_{12} = t_2 - t_1 \approx L_{r11} I_o / (2n_{11}^2 v_{Cc1})$. The energy stored on capacitors C_{c1} and C_{c2} is transferred to the output load through (L_{o1} and D_{a1}) and (L_{o2} and D_{a2}), respectively. The *LLC* converters are still worked at resonant mode to delivered power.

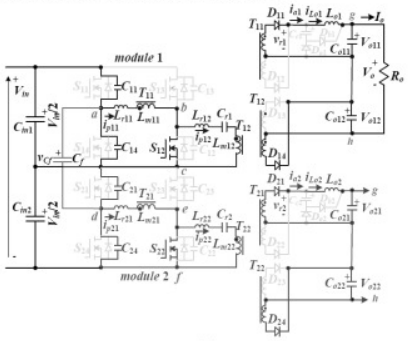
***Stage 3* [t_2 - t_3]:** At time t_2, the rectified currents i_{a1} and i_{a2} decrease to zero. The capacitor currents i_{Cc1}=-i_{Lo1} and i_{Cc2}=-i_{Lo2}. The primary currents i_{p11}=i_{Lm11}≈0 and i_{p21}=i_{Lm21}≈0 in this stage. There is almost no circulating current loss in the primary side of full-bridge converters. In this stage, v_{Lo1}=v_{Cc1}-V_{o11}<0 and v_{Lo2}=v_{Cc2}-V_{o21}<0 so that i_{Lo1} and i_{Lo2} are both decreasing.

***Stage 4* [t_3 - t_4]:** At t_3, switches S_{12} and S_{22} turn off. Since $i_{p12}(t_3)$ and $i_{p22}(t_3)$ are both negative, i_{p12} (i_{p22}) charges C_{12} (C_{22}) and discharge C_{13} (C_{23}). Since the *LLC* converters are working at the inductive load, the primary currents i_{p12} and i_{p22} are lagging to the input fundamental voltages v_{bc} and v_{ef}. Therefore, the ZVS turn-on of S_{13} and S_{23} are easily achieved at t_4.

***Stage 5* [t_4 - t_5]:** At time t_4, the capacitor voltages of C_{13} and C_{23} are decreased to zero. Since $i_{p12}(t_4)$-$i_{p11}(t_4)$<0 and $i_{p22}(t_4)$-$i_{p21}(t_4)$<0, the output diodes of S_{13} and S_{23} conduct. Therefore, the ZVS turn-on of S_{13} and S_{23} are achieved. The rectified currents i_{a1} and i_{a2} increase. Since i_{a1}<i_{Lo1} and i_{a2}<i_{Lo2}, the clamp diodes D_{a1} and D_{a2} conduct. The primary inductor voltages v_{Lr11}=$n_{11}v_{Cc1}$-V_{in}/2<0 and v_{Lr21}=$n_{21}v_{Cc2}$-V_{in}/2<0. The primary currents i_{p11} and i_{p21} both decrease. The *LLC* converters are resonant with v_{bc}=v_{ef}=V_{in}/2. The primary side currents i_{p12} and i_{p22} increase in this stage. The primary currents i_{p11} and i_{p21} decrease until i_{p11}=-i_{Lo1}/n_{11} and i_{p21}=-i_{Lo2}/n_{21}. The duration time in this stage is give as $\Delta t_{45} = t_5 - t_4 \approx L_{r11} I_o / (n_{11} V_{in} - 2n_{11}^2 v_{Cc1})$. In this stage, the primary voltages v_{ab}=v_{de}=-V_{in}/2 in the full-bridge converter and the rectified voltages v_{r1}=v_{Cc1} and v_{r2}=v_{Cc2}. The duty cycle loss at stage 5 is given as $\delta_5 = \Delta t_{45} / T_s = L_{r11} I_o f_s / (n_{11} V_{in} - 2n_{11}^2 v_{Cc1})$.

***Stage 6* [t_5 - t_6]:** At t_5, the rectified currents i_{a1}=i_{Lo1} and i_{a2}=i_{Lo2} so that D_{a1} and D_{a2} are reverse biased. The reflected primary inductance L_{r11}/$(n_{11})^2$ and C_{c1} are resonant with the resonant frequency $f_R = n_{11} / (2\pi\sqrt{L_{r11} C_{c1}})$. Therefore, diodes D_{b1} and D_{b2} conduct in this stage and i_{Lo1} and i_{Lo2} increase. The half of a resonant period 1/($2f_R$) should be less than the minimum effective duty cycle time ($\delta_{eff,min} T_s$/2) in order to reduce the capacitor currents i_{Cc1} and i_{Cc2} to zero before S_{14} and S_{24} are turned off. The rectified voltages v_{r1}=v_{Cc1}+V_{o11} and v_{r2}=v_{Cc2}+V_{o21}. The primary currents i_{p11}=-(i_{Lo1}+i_{Cc1})/n_{11} and i_{p21}=-(i_{Lo2}+i_{Cc2})/n_{21} in this stage.

***Stage 7* [t_6 - t_7]:** At time t_6, i_{a1}=i_{Lo1} and i_{a2}=i_{Lo2} so that diodes D_{b1} and D_{b2} are both reverse biased. The rectified voltages v_{r1}≈V_{in}/($2n_{11}$)>v_{Cc1} and v_{r2}≈V_{in}/($2n_{21}$)>v_{Cc2}. Thus, diodes D_{a1} and D_{a2} are reverse biased. The output inductor voltages v_{Lo1}=V_{in}/($2n_{11}$)-V_{o11}>0 and v_{Lo2}=V_{in}/($2n_{21}$)-V_{o21}>0 so that i_{Lo1} and i_{Lo2} increase. At t_7, S_{14} and S_{24} turn off and the circuit operation for the first half switching period is ended.



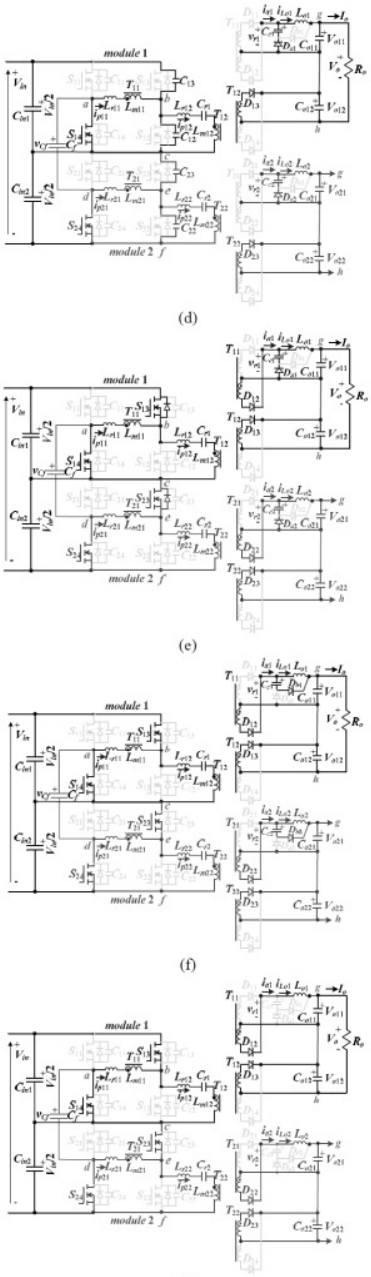


Fig. 4. Operation stages of the proposed converter in the first half of the switching cycle (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6 (g) stage 7.

IV. System Analysis

In the adopted modular converter, each circuit module transfers one-half of the rated power to the output load by both full-bridge converter and full-bridge resonant converter. *LLC* resonant converter is controlled at the constant duty cycle (δ=0.5) and constant switching frequency so that the output voltages V_{o12} and V_{o22} are unregulated. Based on the fundamental frequency analysis, the voltages $V_{o12}=V_{o22}\approx V_{in}/(4n_{12})=V_{in}/(4n_{22})$. The operating switching frequency f_s is close to the series resonant frequency by L_{r12} and C_{r1}, $f_{r1}=1/2\pi\sqrt{L_{r12}C_{r1}}$. Therefore, the primary current of the resonant converter is reduced. Since the resonant converter is worked at the inductive load, the ZVS turn-on of the lagging-leg switches S_{12}, S_{13}, S_{22} and S_{23} is easily achieved from light load. The energy stored on L_{o1} and L_{o2} is used to achieve ZVS turn-on of the leading-leg switches S_{11}, S_{14}, S_{21} and S_{24}. The charge and discharge time of S_{11}-S_{24} can be neglected compared to the other time intervals. Thus, modes 2, 3, 5, 6 and 7 are considered in the following to discuss the circuit characteristics. In stage 6, the average capacitor voltages $V_{Cc1}=V_{in}/(2n_{11})-V_{o11}$ and $V_{Cc2}=V_{in}/(2n_{21})-V_{o21}$. Applying the flux balance on the output inductors L_{o1} and L_{o2}, the output voltages V_{o11} and V_{o21} are obtained as

$$V_{o11}=V_{o21}=\frac{V_{in}}{4n_{11}(1-\delta+\delta_5)}=\frac{V_{in}}{4n_{11}(1-\delta_{eff})} \tag{5}$$

where the effective duty cycle $\delta_{eff}=\delta-\delta_5$, and δ is the duty ratio when S_{11} and S_{12} are in the on-state or S_{13} and S_{14} are in the on-state. The output voltages V_o is given in (6).

$$V_o=V_{o11}+V_{o12}=\frac{V_{in}}{4n_{11}(1-\delta_{eff})}+\frac{V_{in}}{4n_{12}} \tag{6}$$

From (6), the dc voltage gain of the proposed modular dc/dc converter is derived in (7).

$$M_{dc}=V_o/V_{in}=\frac{n_{12}+(1-\delta_{eff})n_{11}}{4n_{11}n_{12}(1-\delta_{eff})} \tag{7}$$

The respective output powers of full-bridge converter and half-bridge resonant converter are expressed as

$$P_{full-bridg}\approx\frac{V_{in}I_o}{4n_{11}(1-\delta_{eff})} \tag{8}$$

$$P_{half\text{-}bridge}\approx\frac{V_{in}I_o}{4n_{12}} \tag{9}$$

Based on the circuit configuration, the voltage rating of S_{11}~S_{24} is limited at $V_{in}/2$. The output inductor current ripple Δi_{Lo1} and Δi_{Lo2} can be obtained in (10).

$$\begin{aligned}\Delta i_{Lo1}=\Delta i_{Lo2}&=(V_{o11}-V_{Cc1})(0.5-\delta_{eff})T_s/L_{o1}\\&\approx(2V_{o11}-\frac{V_{in}}{2n_{11}})(0.5-\delta_{eff})T_s/L_{o1}\end{aligned} \tag{10}$$

The output inductances L_{o1} and L_{o2} can be obtained if the ripple currents Δi_{Lo1} and Δi_{Lo2} are given.

$$L_{o1}=L_{o2}\geq(2V_{o1}-\frac{V_{in}}{2n_{11}})(0.5-\delta_{eff})T_s/\Delta i_{Lo1} \tag{11}$$

Based on the main PWM waveforms in Fig. 2, the theoretical average current and voltage stress of the rectifier diodes D_{11}-D_{24} are

$$i_{D11,\mathrm{av}} = i_{r12,av} = i_{D21,\mathrm{av}} = i_{D22,av} \approx \delta I_o / 2 \quad (12)$$

$$i_{D13,\mathrm{av}} = i_{D14,av} = i_{D23,\mathrm{av}} = i_{D24,av} \approx I_o / 4 \quad (13)$$

$$v_{D11,\mathrm{stress}} = v_{D12,\mathrm{stress}} = v_{D21,\mathrm{stress}} = v_{D22,\mathrm{stress}} \approx V_{in} / n_{11} \quad (14)$$

$$v_{D13,\mathrm{stress}} = v_{D14,\mathrm{stress}} = v_{D23,\mathrm{stress}} = v_{D24,\mathrm{stress}} \approx 2V_{o11} = V_{in} / (2n_{12}) \quad (15)$$

The average current and voltage stresses of the diodes D_{a1}-D_{b2} are expressed as

$$i_{Da1,\mathrm{av}} = i_{Da2,av} = i_{Db1,\mathrm{av}} = i_{Db2,av} \approx (1-2\delta) I_o / 2 \quad (16)$$

$$v_{Da1,\mathrm{stress}} = .. = v_{Db2,\mathrm{stress}} \approx V_{o11} = \frac{V_{in}}{4n_{11}(1-\delta_{eff})} \quad (17)$$

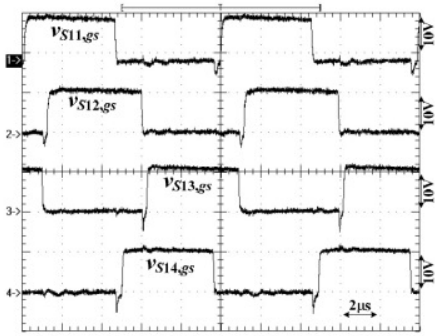


Fig. 5. Measured waveforms of the gating voltages of S_{11}~S_{14} at full load.

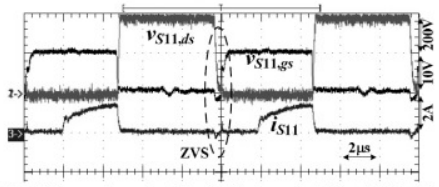


Fig. 6. Measured results of the leading-leg switch S_{11} at 30% load.

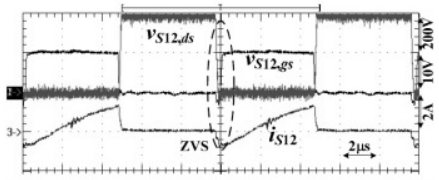


Fig. 7. Measured results of the leading-leg switch S_{12} at 5% load.

V. Experimental Results

Experiments based on a laboratory prototype are presented to show the performance and effectiveness of the proposed modular dc/dc converter. The prototype circuit is realized with the electric specifications: V_{in}=750V~800V, V_o=48V, $I_{o,max}$=40A, $P_{o,rated}$=1920W, and f_s=100kHz (switching frequency). The power ratings of the two half-bridge converters and two full-bridge converters are assumed as 800W and 1200W, respectively. Thus, each resonant converter is rated at 400W and full-bridge converter is operated at 600W rated power. The output current of each resonant converter is I_o/2=40/2=20A. Therefore, the output voltages V_{o12} and V_{o22} are 400W/20A=20V. Fig. 5 gives the experimental waveforms $v_{S11,gs}$-$v_{S14,gs}$ for 100% loads. The gating signals of S_{21}-S_{24} are the same as the gating voltages of S_{11}-S_{14}. The experimental waveforms $v_{S11,gs}$, $v_{S11,ds}$, and i_{S11} at 30% load are illustrated in Fig. 6. Before switch S_{11} is turned on, the drain current is negative to discharge the output capacitor of S_{11}. Thus, the drain voltage can be decreased to zero before the gate voltage is high voltage level. The ZVS turn-on of S_{11} is achieved from 30% load to full load. Fig. 7 shows the experimental waveforms $v_{S12,gs}$, $v_{S12,ds}$, and i_{S12} at 5% load. Since the *LLC* resonant converter and full-bridge converter share the lagging-leg switches, it is clear that the ZVS turn-on of S_{12} is achieved from 5% load to full load. Fig. 8 shows the measured waveforms v_{ba}, v_{bc}, v_{Cr1}, v_{ed}, v_{ef}, v_{Cr2} and i_{p11}~i_{p22} at full load. There are three voltage levels on v_{ba} and v_{ed} and two voltage levels on v_{bc} and v_{ef}. At the freewheeling state, the primary currents i_{p11} and i_{p21} are decreased to zero. Thus, the conduction loss at freewheeling state is removed. The primary currents i_{p12} and i_{p22} are the quasi-sinusoidal currents. Fig. 9 shows the experimental voltage waveforms v_{Cin1}, v_{Cin2} and v_{Cf}. Based on the measured results, three capacitor voltages v_{Cin1}, v_{Cin2} and v_{Cf} are balanced. The measured circuit efficiencies are 92.1%, 94.2%, 95.3% and 93.5% at 480W (25% load), 960W (50% load), 1440W (75% load) and 1920W (full load), respectively.

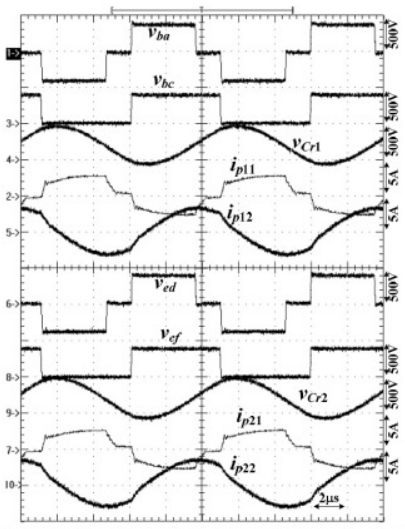


Fig. 8. Measured results of the ac side voltages and primary side currents at full load.

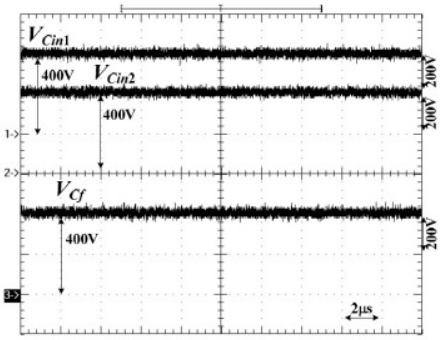


Fig. 9. Measured results of the input split capacitor voltage and flying capacitor voltage at full load.

VI. Conclusion

This paper studies a modular multilevel converter to have the advantages of low voltage stress of switches, wide ZVS range of all switches and low conduction losses at freewheeling state. The series full-bridge converter is adopted at high voltage side to limit the voltage stress of switches at $V_{in}/2$. Therefore, the low turn-on resistance power MOSFETs are used to reduce the conduction losses. *LLC* resonant converter and full-bridge converter share the lagging-leg switch to extend the ZVS range from low load to full load. The primary currents can be reduced to zero at freewheeling state due to a passive snubber circuit is used on the output side. The output voltages of *LLC* converter and full-bridge converter are connected in series. Thus, the output power can be transferred by both converters. The flying capacitor is adopted on the primary side to balance input voltages. Finally, experiments with a laboratory prototype rated at 1920W are presented to show the performance of the proposed circuit.

Acknowledgment

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Analysis of a New Resonant Converter with Auxiliary Windings to Extend Input Voltage Range

B.R. Lin, *Senior Member, IEEE*, J.J. Dai and Y.K. Du
Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin 640, Taiwan

***Abstract*–The resonant converters have been developed for medium-power applications due to the high circuit efficiency and high power density. However, the switching frequency is related to the voltage gain of resonant converter. Therefore, the resonant converter is usually limited at narrow input voltage applications. To overcome this limitation, the auxiliary winding and switch are adopted at the secondary side to provide a high voltage gain under low input voltage case or to extend the hold-up time when AC power is turned off. Thus, the switching frequency variation can be reduced for the wide input voltage case. The operation principle, circuit characteristics and design procedure of the proposed converter are presented in detail. Experiments are provided to verify the effectiveness and demonstrate the circuit performance.**

Keywords—power converters; hold-up time; ZVS.

I. Introduction

In modern power converters for data storage systems, server systems or telecommunication systems, compact size and high circuit efficiency are usually demanded. Two stage AC/DC converters are normally adopted to draw a sinusoidal line current from utility line and provide a stable DC output voltage against the line voltage and load current variations. The boost-type bridge or bridgeless power factor correctors are adopted in the front stage to provide a stable DC bus voltage for second stage use and meet the international harmonic standard EN61000-3-2 class-D. Zero-voltage switching (ZVS) DC/DC converters are normally used in the second stage to provide a stable DC output voltage for server and data storage power units. Full-bridge converters [1]-[4] with phase-shift pulse-width modulation (PS-PWM) scheme are adopted for power level more than 1kW. However, the drawbacks of the phase-shift full-bridge converter are high circulating current, narrow ZVS range of lagging-leg switches and high voltage oscillation on rectifier diodes. Thus, the circuit efficiency is low especially at light load condition. Half-bridge or full-bridge *LLC* resonant converters [5]-[8] can be used in the power level less than 1kW with the functions of full range of ZVS for power switches and zero-current switching (ZCS) for rectifier diodes if the switching frequency is less than the series resonant frequency. Therefore, the high circuit efficiency can be achieved for server systems. However, the hold-up time [9]-[10] is demanded for the data storage and server systems to allow AC power dropout with one cycle of line frequency. During the hold-up time, the energy stored in the high voltage DC bus capacitor is released to keep the output capacitor at the desired voltage level by variation the duty cycle (PWM scheme) or switching frequency (PFM) of the DC/DC converters. Therefore, it is better that the DC/DC converter can work at a wide input voltage range to reduce the cost and power density. The low inductor ratio between the magnetizing inductance and series resonant inductance is selected in *LLC* resonant converter to achieve a high voltage gain at hold-up time stage. The low magnetizing inductor will result in high circulating current losses and reduce the circuit efficiency. To solve the hold-up time problem, the additional boost converter with backup capacitor [10] is used to keep high DC bus voltage stable. The additional power switches in the secondary side [11] and the additional hold-up circuit in the primary side [12] have been proposed in the full-bridge converters to extend the hold-up time and increase the circuit efficiency. However, the control scheme in these hold-up time circuits is very complicated and it is not easy to be implemented using the commercial analog PWM IC.

A new *LLC* series resonant converter with additional secondary windings is presented to provide high voltage gain under low input voltage case (AC power off) for server or data storage system applications. The proposed converter has the advantages of wide input voltage range, less switching frequency variation range, ZVS turn-on of all switches and possible ZCS turn-off of rectifier diodes and longer hold-up time when AC power is off. The low inductance ratio used in conventional *LLC* converter to obtain high voltage gain is not necessary needed in the proposed converter. Thus, the high circulating current drawback in conventional *LLC* converter can be improved. An input voltage detector circuit is used to select the secondary winding turns in order to obtain the proper voltage gain with narrow switching frequency variation. The circuit diagram, operation principle and circuit characteristics are discussed in detail. Finally, experiments with an 1000W prototype circuit are provided to demonstrate the circuit performance.

II. Circuit Diagram

Figs. 1(a) and 1(b) give the circuit diagram of the conventional half-bridge and full-bridge *LLC* resonant converter for medium power applications. The advantages of the *LLC* converter are wide ZVS range of power switches and possible ZCS operation of rectifier diodes when the switching frequency is less than the series resonant frequency by L_r and C_r. However, the drawback of conventional resonant converter is wide switching frequency variation if the wide input voltage range is necessary. To overcome this problem, the low inductor ratio (the magnetizing inductance versus resonant inductance) and quality factor are usually adopted to obtain high voltage conversion gain under the minimum input voltage case. The low inductor ratio will result in high circulating current losses at the primary side

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so that the circuit efficiency is decreased. Fig. 2 gives the circuit diagram of the proposed resonant converter with wide input voltage operation and less switching frequency variation. V_{in} and V_o are input voltage and output voltage, respectively. S_1-S_4 are MOSFETs. C_{S1}-C_{S4} are the output capacitances of S_1-S_4, respectively. C_r and L_r are the series resonant capacitor and resonant inductor, respectively. D_1-D_4 are the rectifier diodes. T is the isolated transformer with primary winding turns N_p and two secondary turns N_{s1} and N_{s2}. S_a is a power switch. When input voltage is at high voltage level, S_a is turned off. On the other hand, S_a is turned on if the input voltage V_{in} is at low voltage level. C_o is output filter capacitor and R_o is load resistance. Frequency modulation scheme is adopted to regulate output voltage. S_a is turned on to increase the DC voltage gain so that the wide input voltage can be used in the proposed converter with less switching frequency variation. Based on the resonant behavior during the transition interval, power switches S_1-S_4 are all turned on at ZVS. Since the resonant frequency is higher than the switching frequency, the rectifier diodes are all turned off at ZCS. Thus, the reverse recovery loss of rectifier diodes is removed.

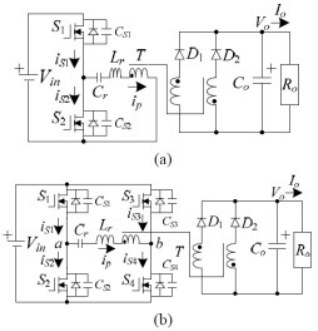


Fig. 1. Circuit diagram of the conventional *LLC* resonant converter (a) half-bridge resonant converter (b) full-bridge converter.

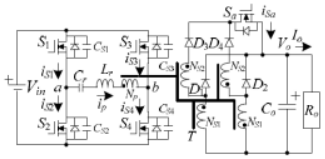


Fig. 2. Circuit diagram of the proposed resonant converter with wide input voltage range and less frequency variation.

III. Operation Principles

Fig. 3(a) shows the equivalent circuit diagram when input voltage is operated at nominal input voltage case (or high voltage level). Switch S_a is turned off. The secondary rectified voltage $|v_{Ns1}|=V_o$. The DC voltage gain of the proposed converter is equal to $N_pV_o/(N_{s1}V_{in,nom})$. When input voltage is decreased to minimum voltage level or low voltage level such as hold-up time case, the switch S_a is turned on (Fig. 3(b)). Thus, the DC voltage gain of the proposed converter equals $N_pV_o/[(N_{s1}+N_{s2})V_{in,low}]$. Compared to the conventional resonant converter with the voltage gain $N_pV_o/(N_sV_{in,low})$ at low voltage case, the proposed converter has much less voltage gain. That means the large inductor ratio or high quality factor can be used in the proposed converter. Therefore, the proposed converter has less circulating current losses and narrow switching frequency variation or longer hold-up time.

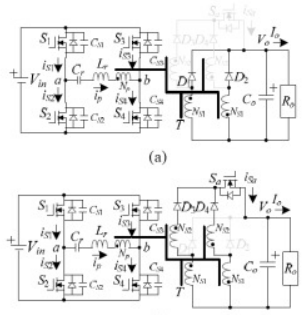


Fig. 3. Equivalent circuit of the proposed converter operated at (a) high input voltage range (b) low input voltage range.

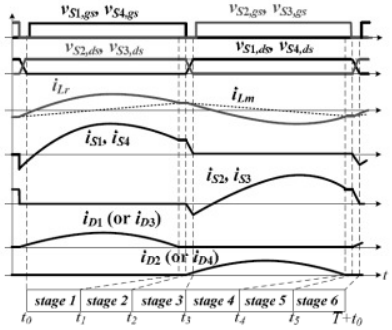


Fig.4. Main PWM waveforms of the proposed converter.

Each switch in the proposed converter is turned on with a 50% duty ratio. Therefore the output voltage regulation is controlled by a frequency modulation technique. All of the active switches are ideal and have the same output capacitance (C_{S1}=C_{S2}=C_{S3}=C_{S4}=C_{eq}). Fig. 4 gives the key waveforms in a switching cycle. There are six operating stages for each switching period when the switching frequency is less than the series resonant frequency. The equivalent circuits for each of the operating stages are shown in Figs. 5 and 6 for the nominal input voltage and the hold-up time case (low input voltage case), respectively. When input voltage is in the nominal voltage level such as V_{in}=390V, switch S_a is turned off. Then, the DC voltage gain under the nominal input voltage case is $N_pV_o/(N_{s1}V_{in,nom})$. Prior to t_0, only rectifier diode D_1 conducts.

***Stage* 1 [t_0 - t_1]:** Since i_p<0, C_{S1} and C_{S4} are discharged to zero voltage at time t_0. Therefore, switches S_1 and S_4 are turned on at this moment to achieve ZVS. The voltage $v_{ab}=V_{in}$. In this stage, the primary current i_p>i_{Lm} so that diode D_1 conducts. The magnetizing voltage $v_{Lm}=n_1V_o$ where $n_1=N_p/N_{s1}$. Thus, the magnetizing current i_{Lm} increases linearly. Resonant inductor L_r

and resonant capacitor C_r are resonant with the applied voltage V_{in}-n_1V_o.

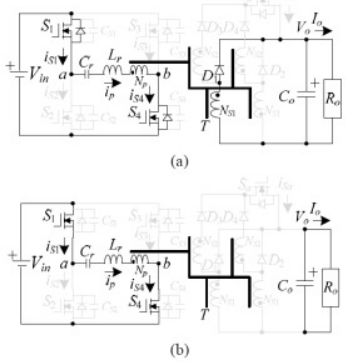
***Stage* 2 [t_1 - t_2]:** At t_1,, the primary current i_p=i_{Lm}. Therefore, the diode current i_{D1} is decreased to zero and D_1 can be turned off at ZCS. The reverse recovery loss of D_1 is removed. In this stage, C_r, L_r and L_m are resonant. Since L_m>>L_r, the primary current i_p is almost constant in this stage.

***Stage* 3 [t_2 - t_3]:** At t_2, S_1 and S_4 are turned off and the rectifier diode D_2 conducts. Since $i_p(t_2)$>0, C_{S2} and C_{S3} are discharged and C_{S1} and C_{S4} are charged. If the energy stored in L_r and L_m is greater than the energy stored in C_{S1}~ C_{S4}, then C_{S2} and C_{S3} can be discharged to zero voltage at time t_3 and the anti-parallel diodes of S_2 and S_3 conduct.

***Stage* 4 [t_3 - t_4]:** At time t_3, C_{S2} and C_{S3} are discharged to zero voltage. Since $i_p(t_3)$ is positive, the anti-parallel diodes of S_2 and S_3 conduct. Therefore, S_2 and S_3 can be turned on at this moment to achieve ZVS. In this stage, v_{ab}=-V_{in}, diode D_2 conducts, the magnetizing voltage v_{Lm}=n_1V_o, and i_{Lm} decreases linearly. Resonant inductor L_r and capacitor C_r are resonant with the applied voltage -V_{in}+n_1V_o and the primary current i_p decreases. Energy is transferred from V_{in} to R_o through transformer T and diode D_2.

***Stage* 5 [t_4 - t_5]:** At t_4, the primary current i_p=i_{Lm}. Thus, the diode current i_{D2} is decreased to zero and D_2 can be turned off at ZCS. The reverse recovery loss of D_2 is removed. In this stage, C_r, L_r and L_m are resonant. Since L_m>>L_r, the primary current i_p is almost constant in this stage.

***Stage* 6 [t_5 – t_0+T_s]:** At time t_5, S_2 and S_3 are turned off. Since $i_p(t_5)$<0, C_{S1} and C_{S4} (C_{S2} and C_{S2}) are discharged (charged). If the energy stored in L_r and L_m is greater than the energy stored in C_{S1}~ C_{S4}, then C_{S1} and C_{S4} can be discharged to zero voltage at time t_0+T_s and the anti-parallel diodes of S_1 and S_4 conduct. Then, the circuit operations in a switching period are completed. When input voltage is drop in the hold-up stage. Switch S_a is controlled at the on-state to decrease the necessary voltage gain and reduce the switching frequency variation. The DC voltage gain under the hold-up stage is N_pV_o/[$(N_{s1}$+$N_{s2})V_{in,low}$]. Fig. 6 shows the equivalent operation stages of the proposed converter at hold-up stage. The operation behaviors at hold-up stage are similar to the nominal stage with the secondary winding turns N_{S1}+N_{S2} instead of N_{S1}.



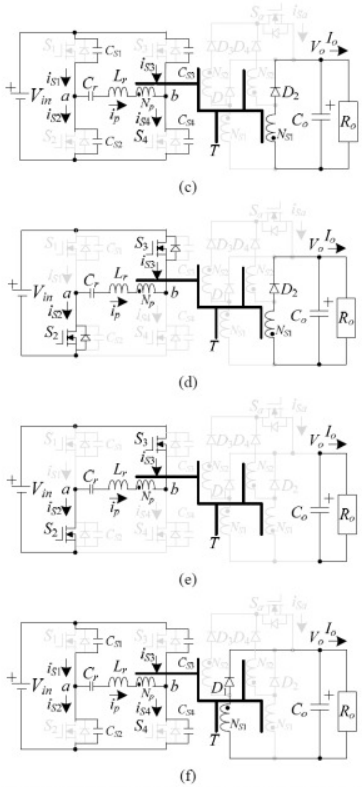
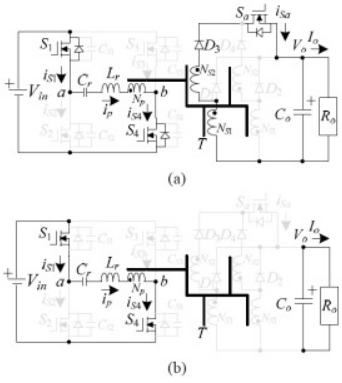


Fig. 5. Operation stages of the proposed converter at high input voltage range (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6.



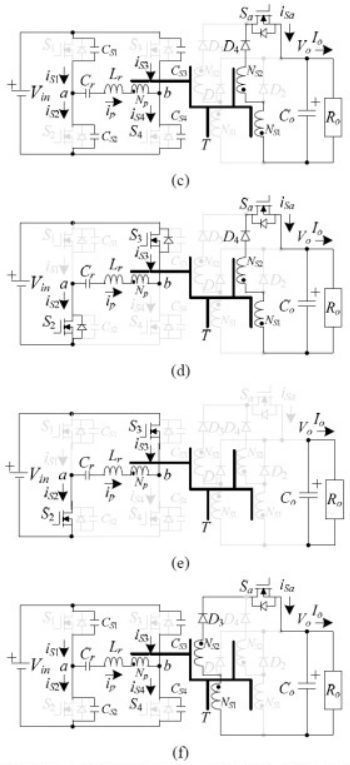


Fig. 6. Operation stages of the proposed converter at low input voltage range (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6.

IV. System Analysis

The charge and discharge times in stages 3 and 6 are much less than the other stages. Thus, the circuit behaviors in stages 3 and 6 can be neglected in the steady state analysis. In stages 1 and 4, the converter is resonant at series resonant frequency $f_r = 1/2\pi\sqrt{L_r C_r}$. However, the converter is resonant at frequency $f_m = 1/2\pi\sqrt{(L_r + L_m)C_r}$ in stages 2 and 5. The power flow through the resonant tank is related to the switching frequency. All of the harmonics of the switching frequency are neglected in the following analysis. Based on the fundamental frequency analysis of the series resonant converter, the AC voltage gain of the resonant tank is given as:

$$|G_{ac}(f_s)| = \frac{V_{Lm}}{V_{ab,f}} = 1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2 + Q^2(\frac{f_s}{f_r} - \frac{f_r}{f_s})^2} \quad (1)$$

Where $R_{ac} = 8n^2 R_o/\pi^2$, $f_r = 1/2\pi\sqrt{L_r C_r}$, $Q = \sqrt{L_r/C_r}/R_{ac}$, $k=L_r/L_m$, $n=N_p/N_{S1}$ (when S_a is off) or $N_p/(N_{S1}+N_{S2})$ (when S_a is on) and f_s is the switching frequency. The AC voltage gain $G_{ac}(f_s)$ is related to the switching frequency in (1). Therefore, the output voltage V_o can be regulated by the variation of the switching frequency f_s. The DC voltage gain of the proposed converter is expressed as

$$G_{dc} \approx \frac{n(V_o + V_D)}{V_{in}} \quad (2)$$

where V_D is the voltage drop on D_1-D_4. The turns ratio of transformer can be obtained from (1) and (2) if the inductor ratio k, quality factor Q, switching frequency f_s, series resonant frequency f_r and input voltage V_{in} are given. If the operated switching frequency $f_s \leq f_r$, then the magnetizing current variation of transformer T is obtained in (3).

$$\Delta i_{Lm} = \frac{n(V_o + V_D)}{2L_m f_r} = 2I_m \quad (3)$$

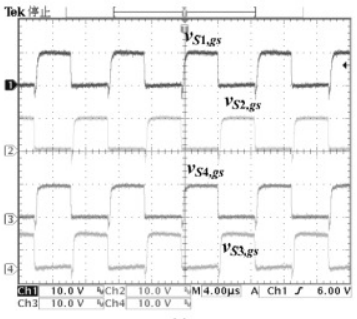
where I_m is the peak current of magnetizing inductor. Therefore, the peak magnetizing inductor current I_m is obtained as:

$$I_m = \frac{n(V_o + V_D)}{2L_m f_r} \quad (4)$$

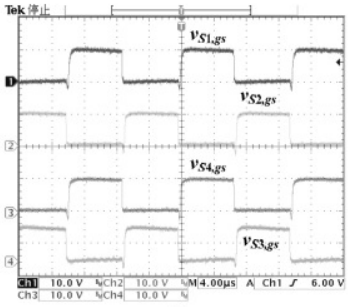
The voltage rating of switches S_1-S_4 is limited to input voltage V_{in}. Due to the resonant tank by L_r, L_m and C_r are operated at the inductive load. The ZVS operation of switches S_1-S_4 is naturally achieved.

V. Experimental Results

In this section, the test results are provided to demonstrate the performance of the proposed converter with wide input voltage range and less switching frequency variation to extend the hold-up time when AC power is off. A 1kW rated power prototype was implemented in the laboratory. The output voltage and the load current are 48V and 20.8A. The input voltage range is from 200V to 400V. The selected series resonant frequency f_r is 90kHz and the inductance ratio $k=L_r/L_m$ is selected as 0.25. When input voltage is less than 280V, the power switch S_a is turned on to provide high voltage gain in order to reduce the switching frequency variation. The turns ratio N_p:N_{s1}:N_{s2}=42:6:6. The selected series resonant inductance L_r and resonant capacitance C_r are 120μH and 25nF, respectively. The magnetizing inductance L_m of transformer T is 480μH. The power MOSFETs S_1-S_4 are FQA24N50. The rectifier diodes D_1-D_4 are MBR40200PT. The PMOS IRF9540N is adopted for S_a. The output capacitance C_o is 2200μF.

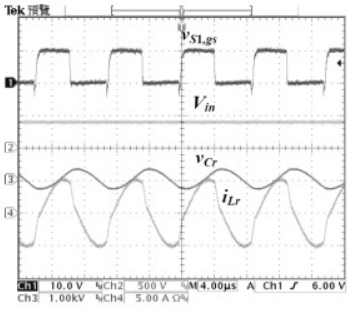


(a)

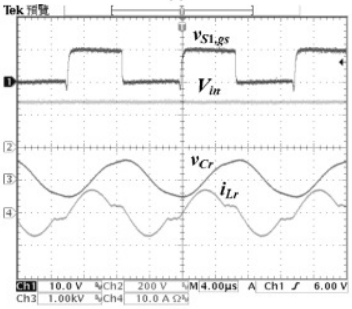


(b)

Fig. 7. Measured gate voltages of S_1-S_4 at full load and (a) V_{in}=400V (b) V_{in}=280V.



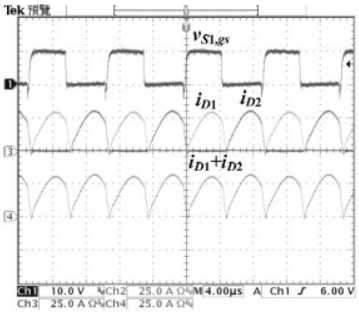
(a)



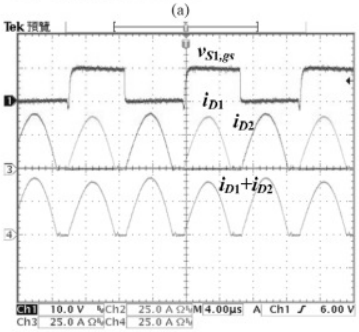
(b)

Fig. 8. Test waveforms of gate voltage $v_{S1,gs}$, input voltage V_{in}, resonant capacitor voltage v_{Cr} and resonant inductor current i_{Lr} at full load and (a) V_{in}=400V (b) V_{in}=280V.

Since the adopted resonant converter is operated at the inductive load, the power switches S_1-S_4 are operated at ZVS turn-on from light load to full load within wide range of input voltage. In the normal stage, the input voltage variation is from 280V to 400V and the power switch S_a is off. Fig. 7 shows the measured gate voltages of S_1-S_4 at 400V and 280V input case and full load. Fig. 8 gives the test waveforms of gate voltage $v_{S1,gs}$, input voltage V_{in}, resonant capacitor voltage v_{Cr} and resonant inductor current i_{Lr} at full load and different input voltage case. It is clear to see that the switching frequency of the converter is less than the series resonant frequency when V_{in}=280V. Fig. 9 illustrates the experimental waveforms of the rectifier diode currents at full load. The rectifier diodes are turned off at zero-current switching and the reverse recovery current losses of fast recovery diodes are improved at V_{in}=280V case. In the hold-up stage, the power switch S_a is turned on to provide high DC voltage gain. The input voltage can be worked from 200V at hold-up time stage and extend the hold-up time when AC power is off. Fig. 10 shows the measured results of the proposed converter under the hold-up stage (V_{in} is decreased) at 200V input case and full load. Fig. 11 gives the measured results of the hold-up time operation waveforms with and without the second secondary winding turns N_{S2} under the full load condition. There is a 30ms hold-up time in the conventional resonant converter with minimum input voltage 320V. In the proposed converter, power switch S_a is turned on to provide high DC voltage gain and extend the hold-up time when the input voltage is decreased to 280V under the hold-up stage. The hold-up time in the proposed converter at full load condition can be extended to 50ms. Therefore, the proposed converter has wide input voltage range (200V~400V) and longer hold-up time. The measured circuit efficiencies of the proposed converter at V_{in}=400V are 92.8%, 94.6% and 93.3% under 20%, 50% and 100% loads, respectively.



(a)



(b)

Fig. 9. Experimental waveforms of the rectifier diode currents at full load (a) V_{in}=400V (b) V_{in}=280V.

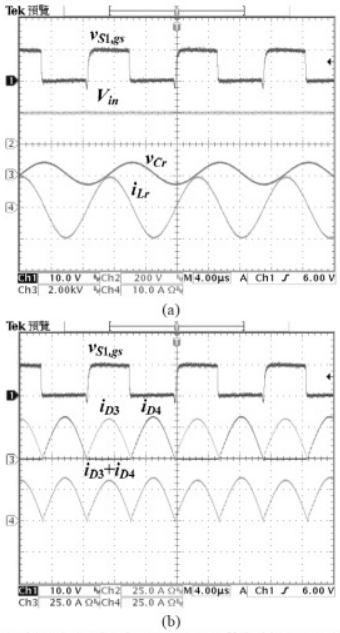


Fig. 10. Measured results under the AC power off (hold-up stage) at 200V input case and full load (a) $v_{S1,gs}$, V_{in}, v_{Cr} and i_{Lr} (b) $v_{S1,gs}$, i_{D3}, i_{D4} and $i_{D3}+i_{D4}$.

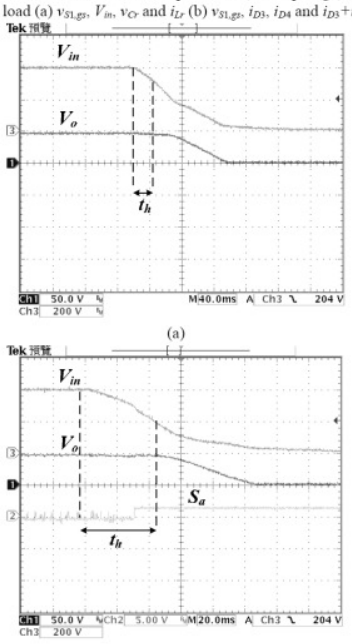


Fig. 11. Waveforms of the hold-up time operation at full load (a) conventional LLC resonant converter without N_{S2} windings (b) the proposed converter.

VI. Conclusion

A new resonant converter is presented solve the hold-up time problem and extend input voltage range. The LLC series resonant converter with additional secondary windings is proposed to extend the hold-up time problem. At hold-up time stage, the higher secondary winding turns are used to obtain higher voltage gain so that the switching frequency variation range can be reduced. Thus, the adopted converter can be operated at the wide input voltage range without using very low inductance ratio and low quality factor in the conventional LLC converter. Thus, the circuit efficiency in conventional LLC converter can be improved in the proposed converter. The validity of the proposed converter was verified by experiments with 1000W prototype.

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