出國報告（出國類別：其他-國際會議）

參加「二〇一五年IEEE INTELEC國際學術研討會」出國報告

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出國期間：104 年 10 月 18 日至 104 年 10 月 23 日

摘要

10 月 18~23 日出席二〇一五年 IEEE-INTELEC 國際會議，參加此會議目的是向各國電力電子專家學者討論電源轉換器之應用趨勢與介紹個人在電力電子研究成果，學習各國電源轉換技術在電信方面之應用並討論高效率電源轉換器術與再生能源之趨勢。學習與會學者與業界工程師在電力電子技術、能源技術、電信電源技術與再生能源應用發展趨勢。研討會期間與國外專家學者互討論能源轉換技術等相關問題，以提升在電力電子方面的深度與廣度。研討會中，針對筆者發表數種不同方法的高壓直流電源轉換器架構來實現高效率及低損耗的電源供應器有深入之討論與答辯，此電路架構都具有高效率電路等優點，最後利用硬體電路實現來證明所提新型高壓直流電源轉換器之實用性與優越性能。此次參加 IEEE-INTELEC 研討會獲得很多國外之研究成果，也詳細向國外學者介紹台灣之研究績效。

目次

一、 目的

參加二〇一五年IEEE-INTELEC國際通信能源會議之主要目的為1.發表個人近幾年在高效率能源轉換之研究成果，2.了解各專家學者與研究單位的研究方向與成果，3.與國際能源轉換專家學者廣泛討論高效率電源轉換技術與科技趨勢，4.向各國際學者介紹台灣在高效率電源轉換器技術研究之成果。

二、 過程

二〇一五年IEEE-INTELEC國際通信能源會議在日本/大阪召開，會議時間自10月18日至10月22日。主辦單位為IEEE電力電子協會，承辦單位為長崎大學。INTELEC國際通信能源會議是每年舉辦一次的國際學術研討會，每年會議在世界各國家舉辦。此次研討會投稿篇數為約400篇，投稿全文經多位審稿者無記名審查，通過審查共有262篇論文於會議中發表，文章接受率約為60%。會議中安排有四場專業演講，五場主題演講，會議內容共有44個時段之論文發表分別於10/19至10/22舉行。10/19日至10/22日參加各場次之論文發表會，筆者於研討會會中發表一篇論文:

Analysis and Implementation of a Hybrid ZVS Converter

筆者論文中發表一種不同方法之高效率混合式直流轉換器架構，此電路對實現高效率及低損耗的電源供應器有深入討論，此電路架構具有零電壓切換技術，文章中利用硬體電路實現結果來證明所提新型電力轉換器之實用性與優越性能，此篇文章獲得日本學者之興趣，有熱烈討論與互相交流。個人在會議過程中參加了高效率電源轉換器、再生能源、通訊用電源技術與高功率電源技術等各項論文發表場次，會議中有約 10 次提出對於該論文研究成果之建議，也都得到各作者之說明與答辯，會後也與各作者有近一步之互動與討論，大家也互相交換名片做為將來互相書信與郵件通信用，也對台灣在此領域之研究成果有充分之了解。該會議為一有關之電信用電源技術國際研討會，會議內容包含能源技術、電信電源技術與再生能源應用。

三、 心得

IEEE-INTELEC 國際通信能源會議為全世界有關電力電子及能源技術相關研究方面重要會議之一。本次會議共有 262 篇論文。台灣有很多師生參與，包括台北科技大學電機系劉邦榮教授及賴炎生教授、台科大電子系邱煌仁教授、成功大學電機系梁從主教授及國內私立大學其他教授等共十多位人員參加。為提高台灣之學術地位及能見度，仍需科技部與教育部繼續支持。在本次的會議中可以看出論文品質提升，在會議中能認識其他國家的人士，彼此能交換心得，對於開拓視野、提升研究品質有莫大的幫助。會中與各國專家學者交換意見，獲益良多。茲將出席本次會議心得分述如下：

1. 台灣學者在研究品質上與各國相比較，表現很好。
2. 會中與各國專家學者交換高效率電源轉換器與再生能源技術，獲益良多。

3. 與中國、日本及韓國學者在大會上廣泛互動與討論研究方向，作為將來合作之機會。
4. 此次會議中較多研究論文發表集中通訊用能源轉換技術，利用高效能轉換器技術讓整體電源技術之效率提升，利用智慧型控制理論，增加實用性之產品應用。
5. 雲端電源技術之發展，在此次研討會中也是被討論主題之一。

四、 建議事項

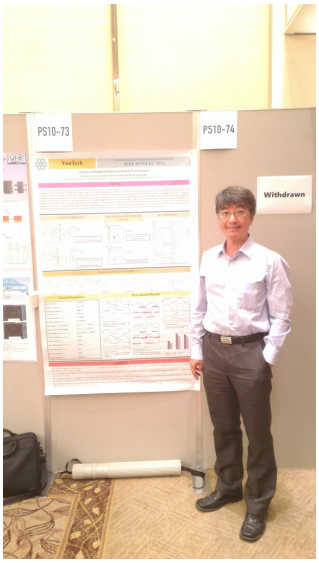
IEEE-INTELEC 國際通信能源會議為 IEEE 有關通信能源轉換相關研究方面重要的國際會議，所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對工業升級及發展高科技所需的高效率電源及驅動系統之發展，均有相當的影響。由於參與類似的學術性會議非常重要，故有以下建議:

1. 鼓勵國內學者積極參與此類型之國際學術會議。
2. 政府應對此領域之研究多加補助。

五、 附錄

發表論文資料。

大會註冊會場



論文發表現場

Analysis and Implementation of a Hybrid ZVS Converter

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***Abstract*—A new hybrid zero voltage switching (ZVS) three-level and half-bridge DC/DC converter is presented to achieve the functions of low voltage stress of switches, low circulating current during the freewheeling interval, wide ZVS range of lagging-leg switches, low output inductor and energy transfer within the whole switching period. The proposed converter includes a three-level phase-shifted pulse-width modulation converter and an un-regulated half-bridge converter. A resonant capacitor is added in conventional three-level DC/DC converter to reduce the circulating current loss to zero during the freewheeling interval. Half-bridge converter, shared the same lagging-leg switches of three-level converter, is used to extend the ZVS range of lagging-leg switches. The secondary windings of two converters are connected in series to generate two positive voltage levels at the rectified voltage instead of one positive voltage and zero voltage. Hence, the output inductance of three-level converter can be reduced. Energy transfers from input to output load through half-bridge converter during the whole switching period and through three-level converter during the active mode operation. Experiments based on a 1440W prototype are provided to validate the theoretical analysis and demonstrate the effectiveness of the proposed converter.**

I. INTRODUCTION

For modern industry power units with high frequency link, switching converters with high power density and high conversion efficiency have been developed to reduce the environmental impacts and meet power quality demands. For medium power applications, three-phase bridge or bridgeless power factor correctors (PFC) and high frequency link three-level DC/DC converters are normally adopted to provide a stable low output voltage with high output current such as battery chargers, server power units [1] or telecommunication power units [2]. Boost converters with diode bridge or bridgeless topologies [4]-[6] have been developed in the front stage to have the functions of a stable DC bus voltage, low line harmonic currents and high input power factor. The rear stage is a high frequency link three-level DC/DC converter [7]-[11] for output voltage regulation and galvanic isolation. Phase-shift pulse-width modulation (PWM) is used to regulate the output voltage. The main disadvantages of phase-shift three-level converter are that the lagging-leg switches have narrow range of zero voltage switching (ZVS) operation due to the limited energy stored in primary leakage inductance and high circulating current losses on the primary side during the freewheeling interval. The large leakage inductance [12] or external resonant inductance [4] is adopted on the primary side to extend the ZVS range of lagging-leg switches. But the large leakage inductor increases duty cycle loss and also decreases the effective duty cycle on the secondary side. Auxiliary circuits in [13]-[14] are added on the primary side to have wide ZVS load range. However, power losses of auxiliary circuits decrease total circuit efficiency.

A soft switching three-level converter integrated with a half-bridge converter in parallel is presented. A resonant capacitor is adopted in the three-level converter to reduce the primary current to zero during the freewheeling interval. Thus, the conduction losses on the primary side can be reduced. Due to the three-level converter and half-bridge converter shared the lagging-leg switches, the lagging-leg switches can be operated at ZVS from full load range and the transformer turns ratio of three-level converter is increased. The larger turns ratio can reduce the voltage stress of rectifier diodes and result in a reduction of secondary conduction losses. The secondary windings of two converters are connected in series so that a positive rectified voltage is generated instead of a zero voltage. Hence, the output filter inductor size is reduced. Finally, experiments with a 1440W prototype circuit are provided to validate the theoretical analysis and effectiveness of the proposed converter.

II. CIRCUIT DIAGRAM

The circuit diagram of conventional three-phase AC/DC modulation converters is shown in Fig. 1(a). The front stage is a three-phase power factor corrector (PFC) with bridge or bridgeless topology to achieve the functions of unity power factor, low total harmonic distortion and constant DC bus voltage. The second stage is a three-level DC/DC converter to have the functions of ZVS turn-on for switches, electric isolation and stable output voltage against load current variation. The phase-shift pulse-width modulation is usually adopted to regulate output voltage. However, the large circulating current during the freewheeling interval, narrow range of ZVS turn-on for lagging-leg switches and large current ripple on the output inductor are the main drawbacks of conventional three-level DC/DC converter.

Fig. 1(b) shows the circuit diagram of the proposed DC/DC converter. The main proposed converter includes one three-level DC/DC converter and one half-bridge converter. The lagging-leg switches are shared by both three-level converter and half-bridge converter. The half-bridge converter

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is operated at fixed 0.5 duty cycle of lagging-leg switches to extend the ZVS range of lagging-leg switches. The resonant capacitor C_r in three-level converter can help the primary current to reduce to zero during the freewheeling interval. Hence, the circulating current loss can be improved. The secondary windings of two converters are connected in series and the rectified voltage v_r at secondary side is positive instead of zero during the freewheeling period. Thus, the voltage across the output inductor is reduced and the inductor current ripple is also decreased. The voltage stress of S_1-S_4 is limited at $V_{in}/2$. The half-bridge converter, including C_{f1}, C_{f2}, S_2, S_3, T_2, L_{r2}, D_2, D_4 and L_o, is operated as an un-regulated mode with fixed 0.5 duty cycle. The output voltage output of three-level converter, including C_{in1}, C_{in2}, D_a, D_b, C_{f1}, C_{f2}, S_1-S_4, T_1, L_{r1}, C_r, D_1, D_3 and L_o, is regulated with the phase-shift PWM scheme. The center-tapped rectifiers are employed at the secondary side to have one diode conduction loss. The output capacitances of S_1-S_4 and the resonant inductance are L_{r1} resonant at the transition interval to allow switches S_1-S_4 to be turned on at ZVS.

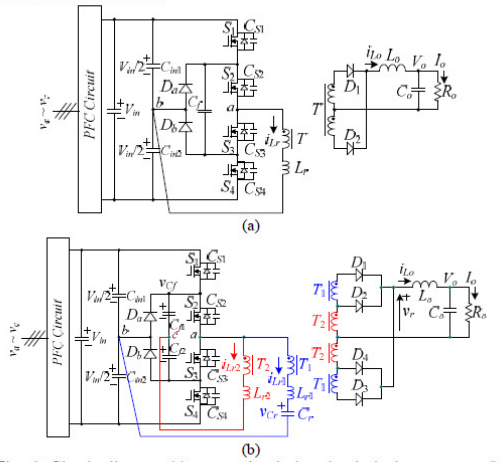

Fig. 1 Circuit diagram (a) conventional three-level dc-dc converter (b) proposed three-level dc-dc converter with less circulating current loss and output inductance.

III. Operation Principle

Phase-shift PWM scheme is adopted to generate the gate voltages of S_1-S_4. The PWM signal of S_2 (S_3) is phase-shifted with respective to the PWM signal of S_1 (S_4). Switches (S_1 and S_4) and (S_2 and S_3) are in the leading-leg and lagging-leg, respectively. S_1 and S_4 operate complementarily with a short dead time to avoid short circuit at high voltage side. In the same manner, the PWM signals of S_2 and S_3 are complementarily with a short dead time. In the following discussions, one assumed that power semiconductors including S_1-S_4, D_a-D_d and D_1-D_6 are ideal, turns ratios of T_1 and T_2 are $n_1=n_{p1}/n_{s1}=n_{p1}/n_{s2}$ and $n_2=n_{p2}/n_{s3}=n_{p2}/n_{s4}$, $C_{S1}=C_{S2}=C_{S3}=C_{S4}=C_{oss}$, and $V_{in1}=V_{in2}=V_{Cf}=V_{in}/2$. The switching waveforms of the proposed converter are given in Fig. 2. The converter has six switching modes during half of switching period. The duty cycle δ is based on the turn-on time of (S_1 and S_2) or (S_3 and S_4). Fig. 3 show the topological circuits during the first half switching period. Prior to t_0, S_1, S_2, D_1 and D_4 are conducting. Inductor current i_{Lr2} is negative.

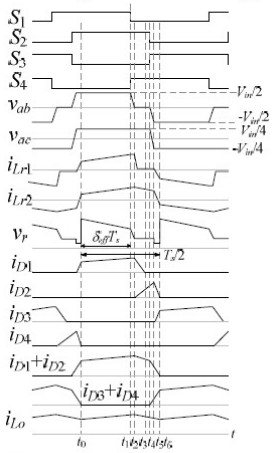

Fig. 2 Key waveforms of the proposed converter.

***Mode* 1 [t_0 - t_1]:** At $t=t_0$, i_{D4} decreases to zero. Since S_1 and S_2 are conducting, energy is transferred from input to output load through three-level converter and half-bridge converter. The AC terminal voltages $v_{ab}=V_{in}/2$ and $v_{ac}=V_{Cf1}=V_{in}/4$. The primary currents $i_{Lr1}=i_{Lo}/n_1$ and $i_{Lr2}=i_{Lo}/n_2$. Capacitor voltage v_{Cr} is obtained as

$$v_{Cr}(t) \approx v_{Cr}(t_0) + \frac{i_{Lo}}{C_r n_1}(t-t_0) \tag{1}$$

The voltage variation of C_r in this mode is given as

$$\Delta v_{Cr} = v_{Cr}(t_1) - v_{Cr}(t_0) = \frac{i_{Lo}}{C_r n_1}(t_1-t_0) = \frac{i_{Lo}\delta T_s}{C_r n_1} \tag{2}$$

The rectified voltage at secondary side is obtained as

$$v_r \approx \frac{V_{in}}{2n_1} - \frac{i_{Lo}}{C_r n_1}(t-t_0) + \frac{i_{Lo}\delta T_s}{2C_r n_1} + \frac{V_{in}}{4n_2} \tag{3}$$

The output inductor voltage $v_{Lo}=v_r-V_o>0$. The output inductor current i_{Lo} increases in this mode.

***Mode* 2 [t_1 - t_2]:** S_1 is turned off at $t=t_1$. Since $i_{Lr1}(t_1)>0$, $i_{Lr2}(t_1)>0$ and D_1 is still conducting, the energy stored in the output inductor L_o is reflected to the primary sides to linearly charge C_{S1} and discharge C_{S4} via capacitors C_{f1} and C_{f2}.

$$v_{CS1} = \frac{(n_1+n_2)i_{Lo}}{2C_{oss}n_1n_2}(t-t_0)\,,\; v_{CS4} = \frac{V_{in}}{2} - \frac{(n_1+n_2)i_{Lo}}{2C_{oss}n_1n_2}(t-t_0) \tag{4}$$

The ZVS turn-on condition of S_4 is approximately given as:

$$(L_{r1}+n_1^2L_o)\times i_{Lr1}^2(t_1) + (L_{r2}+n_2^2L_o)\times i_{Lr2}^2(t_1) \ge C_{oss}V_{in}^2/2 \tag{5}$$

At $t=t_2$, C_{S4} is discharged to zero voltage. Since $i_{S4}(t_2)$ is negative, the anti-parallel diode of S_4 is conducting. The time interval Δt_{12} is obtained as

$$\Delta t_{12} = t_2 - t_1 \approx \frac{V_{in} C_{oss} n_1 n_2}{(n_1 + n_2) i_{Lo,\max}} \quad (6)$$

The dead time t_d between switches S_1 and S_4 must be greater than the time interval Δt_{12} to turn on S_4 at ZVS. The rectified voltage v_r is decreased to $V_{in}/(4n_2)$ at time t_2.

***Mode* 3 [t_2 - t_3]:** Mode 3 starts when v_{CS4}=0 at t_2. Since the switch current $i_{S4}(t_2)$<0, the anti-parallel diode of S_4 is conducting. Hence, S_4 is turned on at ZVS. The AC terminal voltages v_{ab}=0 and v_{ac}=V_{in}/4. The rectifier diodes D_1 and D_2 are conducting to commutate the secondary side current of transformer T_1. L_{r1} and C_r are resonant in this mode to reset the primary current i_{Lr1}. Thus, the circulating current existed in the conventional three-level DC/DC converter is eliminated in the proposed converter so that the conduction losses in the primary side during the freewheeling interval are reduced.

***Mode* 4 [t_3 - t_4]:** At time t_3, the commutation between D_1 and D_2 is completed. Thus, only diode D_2 conducts the load current. The primary side current i_{Lr1} of three-level converter is zero so that no power is transferred through the three-level converter. The primary current of half-bridge converter i_{Lr2}=i_{Lo}/n_2 and energy is transferred from input to output load by the half-bridge converter in this mode. The rectified voltage v_r=$V_{in}/(4n_2)$. The voltage across the output inductor L_o is equal to $V_{in}/(4n_2)$-V_o<0 and the inductor current i_{Lo} decreases in this mode.

***Mode* 5 [t_4 - t_5]:** At t=t_4, S_2 is turned off. Since $i_{Lr2}(t_4)$>0 and D_2 is conducting, the energy stored in the output inductor L_o is reflected to the primary sides to charge C_{S2} and discharge C_{S3} via capacitors C_{f1} and C_{f2}.

$$v_{CS2} = \frac{i_{Lo}}{2C_{oss} n_2}(t - t_0),\ v_{CS3} = \frac{V_{in}}{2} - \frac{i_{Lo}}{2C_{oss} n_2}(t - t_0) \quad (7)$$

The secondary winding voltage of transformer T_2 is decreased. The ZVS turn-on condition of S_3 is approximately given as:

$$(L_{r2} + n_2^2 L_o) \times i_{Lr2}^2(t_1) \geq C_{oss} V_{in}^2 / 2 \quad (8)$$

C_{S3} is discharged to zero voltage at time t_5. Since $i_{S3}(t_3)$ is negative, the anti-parallel diode of S_3 is conducting. The time interval $\Delta t_{45}$is obtained as

$$\Delta t_{45} = t_5 - t_4 \approx \frac{V_{in} C_{oss} n_2}{i_{Lo}} \quad (9)$$

The dead time t_d between switches S_2 and S_3 must be greater than the time interval Δt_{45} to turn on S_3 at ZVS.

***Mode* 6 [t_5 - t_6]:** Mode 5 starts at t_5 when C_{S3} is discharged to zero voltage. Since $i_{S3}(t_5)$<0, the anti-parallel diode of S_3 is conducting and S_3 can be turned on at ZVS. The AC terminal voltages v_{ab}=-V_{in}/2 and v_{ac}=-V_{in}/4. D_2 and D_3 are both conducting to commutate the output inductor current i_{Lo}, and the secondary winding voltages of T_1 and T_2 are $v_{T2,s}$=-0.5$v_{T1,s}$. Since $v_{T1,p} = V_{in}/2 - v_{Cr}(t_5) \approx V_{in}/2 - i_{Lo}\delta T_s/(2C_r n_1)$, the primary side voltage of T_2 can be given as

$$v_{T2,p} = -\frac{n_2 V_{in}}{4n_1} + \frac{n_2 i_{Lo} \delta T_5}{4n_1^2 C_r} \quad (10)$$

The primary current i_{Lr2} is decreased and expressed as

$$i_{Lr2}(t) = n_2 i_{Lo} - (\frac{V_{in}}{4} + \frac{n_2 V_{in}}{4n_1} - \frac{n_2 i_{Lo} \delta T_s}{4n_1^2 C_r})(t - t_5)/L_{r2} \quad (11)$$

Thus, the primary current i_{Lr1} is decreased from zero to -$n_1 i_{Lo}$, and the primary current i_{Lr2} is decreased from $n_2 i_{Lo}$ to -$n_2 i_{Lo}$. At t_6, the commutation between D_2 and D_3 is completed. Thus, only diode D_3 conducts the load current. Then, the circuit operations in the first half switching period are completed.

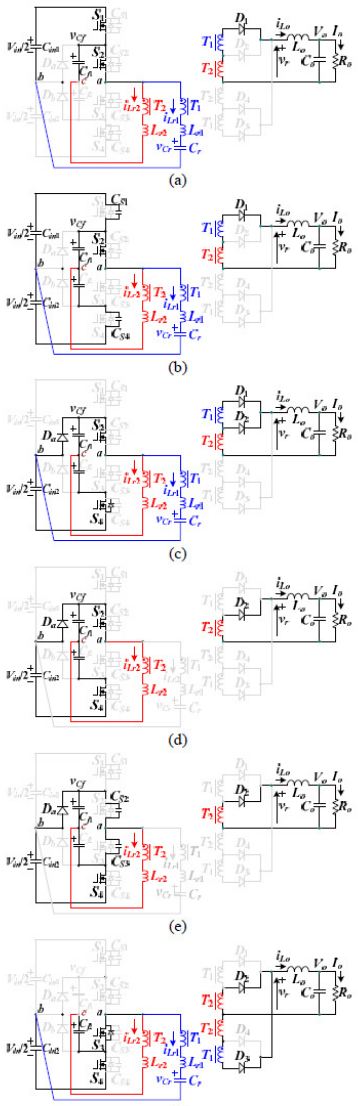

Fig. 3 Operation modes of the proposed converter during the first half switching period (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6.

IV. Circuit Characteristics

A. Voltage Conversion Ratio

From the switching waveforms in Fig. 2, it can be seen that the duration periods of modes 2, 3 and 5 are very narrow compared to the periods of modes 1, 4 and 6. The duty loss in mode 6 is related to the load current and the resonant inductance L_{r1}. This duty loss due to the resonant inductance is existed in both the conventional three-level converter and the proposed converter. Thus, the duty loss is not considered in the following to discuss the voltage conversion ratio. In mode 1, the average rectified voltage $v_r=V_{in}/(2n_1)+V_{in}/(4n_2)$ with the time interval $\delta_{eff}T_s$. On the other hand, the average rectified voltage $v_r=V_{in}/(4n_2)$ in mode 4 with the time interval $(0.5-\delta_{eff})T_s$. Based on the flux balance on output inductor L_o, the output voltage V_o of the proposed converter is derived as

$$V_o = \frac{\delta_{eff}V_{in}}{n_1} + \frac{V_{in}}{4n_2} = (\delta_{eff} + \frac{n_1}{4n_2})\frac{V_{in}}{n_1} \quad (12)$$

However, the output voltage of the conventional three-level converter is given as

$$V_o = \frac{\delta_{eff}V_{in}}{n} \quad (13)$$

From (12) and (13), it is clear to see that the output voltage of the proposed converter is equal to the conventional three-level converter if $n_1/n_2=0$ and $n_1=n$. The comparison of the normalized voltage conversion ratio of the proposed converter and the conventional three-level converter is given as

$$\frac{M_{norm-proposed}(\delta_{eff})}{M_{norm-conventioanl}(\delta_{eff})} = \frac{\frac{n_1V_o}{V_{in}}}{\frac{nV_o}{V_{in}}} = \frac{\delta_{eff}+\frac{n_1}{4n_2}}{\delta_{eff}} \geq 1 \quad (14)$$

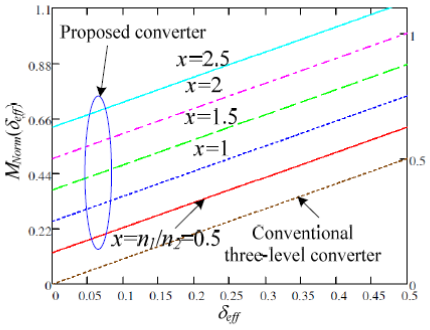

Fig. 4 Normalized gains of the proposed converter and the conventional three-level converter.

Fig. 4 gives the normalized curves of the proposed converter and the conventional three-level converter. It is seen that the gain of the proposed converter is higher than that of the conventional three-level converter. Thus, the turns ratio n_1 of the proposed converter can be larger than that in the conventional three-level converter with the same effective duty ratio. The larger turns ratio n_1 in the proposed converter can reduce the conduction losses on the primary side and also decrease the voltage stress across the rectifier diodes on the secondary side. In the proposed converter, the respective output powers of three-level converter and half-bridge converter are given as

$$P_{three-level} = \frac{\delta_{eff}V_{in}I_o}{n_1},\ P_{half-bridge} = \frac{V_{in}I_o}{4n_2} \quad (15)$$

The percentage of each converter output power versus load power is expressed as

$$\eta_{three-level} = \frac{\frac{\delta_{eff}V_{in}I_o}{n_1}}{\frac{\delta_{eff}V_{in}I_o}{n_1}+\frac{V_{in}I_o}{4n_2}} = \frac{4n_2\delta_{eff}}{4n_2\delta_{eff}+n_1},$$

$$\eta_{half-bridge} = \frac{\frac{V_{in}I_o}{4n_2}}{\frac{\delta_{eff}V_{in}I_o}{n_1}+\frac{V_{in}I_o}{4n_2}} = \frac{n_1}{4n_2\delta_{eff}+n_1} \quad (16)$$

B. Voltage Stress of Rectifier Diodes

From Fig. 3(a), the voltage stress of rectifier diodes can be approximately obtained in (17) and (18) if the voltage spike caused by parasitic elements is neglected.

$$v_{stress,D1} = v_{stress,D3} > \frac{V_{in}}{n_1}+\frac{V_{in}}{2n_2} = \frac{V_o}{\delta_{eff}+\frac{n_1}{4n_2}}(1+\frac{n_1}{2n_2}) \quad (17)$$

$$v_{stress,D2} = v_{stress,D4} > \frac{V_{in}}{2n_1}+\frac{V_{in}}{2n_2} = \frac{V_o}{2(\delta_{eff}+\frac{n_1}{4n_2})}(1+\frac{n_1}{n_2}) \quad (18)$$

In the conventional three-level converter, the voltage stress of rectifier diodes is given as

$$v_{stress,D,conventional} > \frac{V_{in}}{n} = \frac{V_o}{\delta_{eff}} \quad (19)$$

Normally, the maximum effective duty cycle $\delta_{eff,max}<0.5$. Based on (17)-(19), one can obtain that the voltage stress of rectifier diodes D_1-D_4 in the proposed converter is less than that in the conventional three-level converter with the same duty ratio.

C. Output Inductance

In mode 4, the voltage across the output inductor Lo is equal to $V_{in}/(4n_2)$-V_o with the duration period $(0.5-\delta_{eff})T_s$. For the proposed converter, the output inductor value is obtained as

$$L_{o,proposed} > \frac{V_o}{\Delta i_{Lo}} \times \frac{4n_2\delta_{eff}}{n_1+4n_2\delta_{eff}}(0.5-\delta_{eff})T_s \quad (20)$$

For the conventional three-level converter, the output inductor value is given as

$$L_{o,conventional} > \frac{V_o}{\Delta i_{Lo}}(0.5-\delta_{eff})T_s \quad (21)$$

Solving (20) and (21) yields

$$\frac{L_{o,proposed}}{L_{o,conventional}} = \frac{4n_2\delta_{eff}}{n_1+4n_2\delta_{eff}} < 1 \quad (22)$$

It can be seen that the proposed converter has less output inductance compared to the conventional three-level converter with the same current ripple.

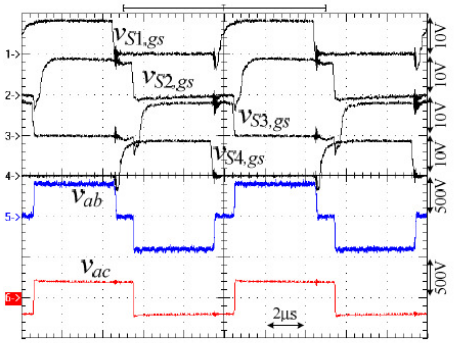

Fig. 5 Measured waveforms ($v_{S1,gs}$, $v_{S2,gs}$, $v_{S3,gs}$, $v_{S4,gs}$, v_{ab}, v_{ac}) of the proposed converter at V_{in}=800V and P_o=1440W (100% load).

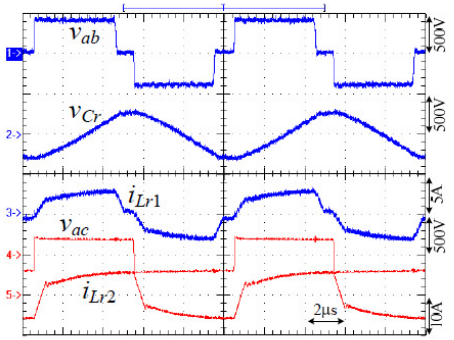

Fig. 6 Measured waveforms (v_{ab}, v_{Cr}, i_{Lr1}, v_{ac}, i_{Lr2}) of the proposed converter at V_{in}=800V and P_o=1440W (100% load).

V. Experimental Verifications

The proposed DC/DC converter is realized with the specifications as input voltage V_{in}=750V-800V, output voltage V_o=48V, maximum load current I_o=30A, and switching frequency f_s=100kHz to verify the performance of the proposed converter. The component parameters of the prototype circuit are S_1-S_4: IRFP460, turns ratio of T_1: 52 turns/4 turns, turns ratio of T_2: 26 turns/4 turns, L_{m1}=2mH, L_{m2}=350µH, L_{r1}=15µH, L_{r2}=15µH, L_o=5µH, C_{in1}=C_{in2}=369µF, C_{f1}=C_{f2}=1µF, C_r=20nF, D_a, D_b: MUR860, D_1-D_4: VF30200C and C_o=4000µF. The measured waveforms of the gating voltages of S_1-S_4 and the AC terminal voltages v_{ab} and v_{ac} of the proposed converter at half load and full load conditions are given in Fig. 5. Fig. 6 illustrates the measured waveforms of the primary side voltages and currents of the proposed converter. It is clear to seen that the circulating current i_{Lr1} of the three-level converter is reduced to zero during the freewheeling interval (v_{ab}=0). Thus, the conduction loss on the primary side during the freewheeling interval is improved compared to the conventional three-level converter. Fig. 7 shows the measured primary side currents and the voltages of the leading-leg and lagging-leg switches at 25% load and full load conditions. Before the leading-leg switch S_1 is tuned on, the primary currents i_{Lr1} and i_{Lr2} are negative to discharge the output capacitor C_{S1} to zero. Thus, the leading-leg switch S_1 is turned on at ZVS. In the same manner, the primary side current i_{Lr1}+i_{Lr2} is negative to discharge the output capacitor C_{S2} to zero before the lagging-leg switch S_2 is turned on. Hence, the lagging-leg switch S_2 is turned on at ZVS. Fig. 8 shows the measured waveforms of v_{ab}, v_r, i_{D1}~i_{D4}, i_{D1}+i_{D2}, i_{D3}+i_{D4} and i_{Lo} at different input voltage cases. Diodes D_2 and D_4 are conducting during the freewheeling interval. Fig. 9 gives the measured circuit efficiencies of the proposed converter at 25%, 50% and 100% loads. The maximum circuit efficiency is 94.8% at 50% load under 750V input voltage.

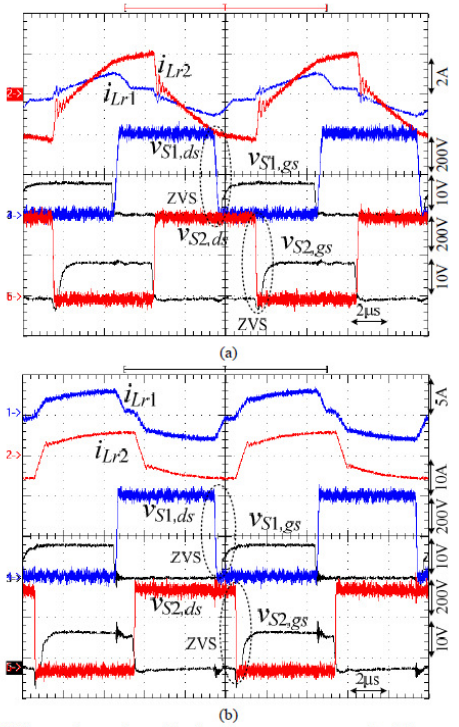

Fig. 7 Measured waveforms (i_{Lr1}, i_{Lr2}, $v_{S1,gs}$, $v_{S1,ds}$, $v_{S2,gs}$, $v_{S2,ds}$) of the proposed converter (a) when V_{in}=800V and P_o=360W (25% load) (b) when V_{in}=800V and P_o=1440W (100% load).

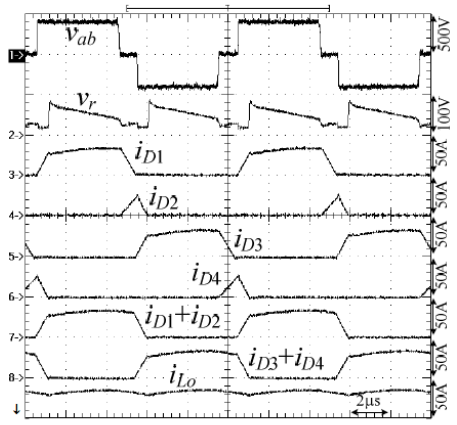

Fig. 8 Measured waveforms (v_{ab}, v_r, i_{D1}~i_{D4}, $i_{D1}+i_{D2}$, $i_{D3}+i_{D4}$, i_{Lo}) of the proposed converter at P_o=1440W.

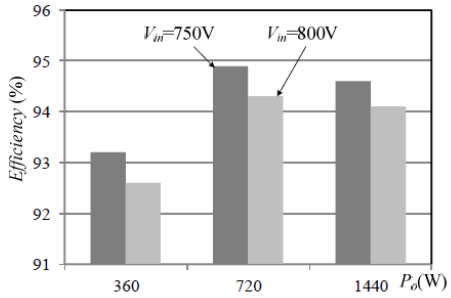

Fig. 9 Measured circuit efficiencies of the proposed converter.

VI. Conclusion

This paper presents a new soft switching three-level DC/DC converter for industry power units. The main advantages of the proposed converter are no circulating current, less conduction losses, wide ZVS range of switches, less voltage stresses on the rectifier diodes and smaller output inductor value. An un-regulated half-bridge converter shares the same lagging-leg switches as the three-level DC/DC converter to extend the ZVS range of lagging-leg switches from light load to full load. The resonant capacitor is adopted in the primary side of three-level converter to reduce the circulating current to zero during the freewheeling interval. Thus, the conduction loss at the primary side of three-level converter in the freewheeling interval is reduced. The secondary sides of two converters are connected in series to generate a positive rectified voltage instead of zero voltage in the conventional three-level converter so that the output inductance is reduced at the same current ripple. Energy is transferred from input to output load within the whole switching cycle through the half-bridge converter. Hence, the proposed converter has more effective energy transfer. The performance of the proposed converter has been verified throughout experiments based on a 1440W prototype circuit. Experimental results confirm the effectiveness of the proposed converter.

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