出國報告（出國類別：其他-國際會議）

參加「二〇一五年IEEE PEDS國際學術研討會」出國報告

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報告日期：104 年 6 月 15 日
出國期間：104 年 6 月 9 日至 103 年 6 月 14 日

摘要

個人出席二〇一五年 IEEE-PEDS 國際會議，此行之主要目的是向各國電力電子專家學者討論電源轉換器之趨勢與介紹國內電力電子之研究成果，了解亞洲各國電源轉換技術並討論高效率電源轉換器術與再生能源之應用趨勢。聆聽各國學者與業界工程師在電力電子技術、馬達製造、能源控制、智慧控制、混合式電動車之研究趨勢與再生能源應用發展趨勢。研討會期間與國外研究學者及專家相互討論能源轉換技術與再生能源新技術等相關問題，以提升個人在電力電子研究方面的深度與廣度。研討會中，針對筆者發表數種不同方法的高壓直流電源轉換器架構來實現高效率及低損耗的電源供應器有深入之討論與答辯，此電路架構都具有零電壓切換技術及高效率電路等優點，此多種電路採用不相同的控制方法在不同運用方面的優點有充分之說明與推論，最後利用硬體電路實現來證明所提新型高壓直流電源轉換器之實用性與優越性能。此次參加 IEEE-PEDS 研討會獲得很多國外之研究成果，也詳細向國外學者介紹台灣之研究績效。

目次

一、 目的

參加二〇一五年IEEE-PEDS電力電子與電動機驅動國際研討會之主要目的為1.發表個人近幾年來之研究成果，2.學習世界專家學者與研究單位的研究方向與成果，3.與國際學者廣泛討論高效率電源轉換技術與科技趨勢，4.向國際專家學者介紹台灣在高效率電源轉換器技術研究之成果。

二、 過程

二〇一五年IEEE-PEDS電力電子與電動機驅動國際研討會在澳洲/雪梨召開，會議時間自6月9日至6月12日。主辦單位為IEEE工業應用協會新加坡分會，協辦單位為IEEE澳洲雪梨區分會，承辦單位為昆士蘭科技大學。PEDS電力電子與電動機驅動國際學術研討會是每兩年舉辦一次的國際學術研討會，每年會議在亞洲各國家舉辦(2017年會議將於六月於夏威夷舉辦)。此次研討會投稿篇數為450篇，投稿全文經三位審稿者無記名審查，通過審查共有200篇論文於會議中發表，文章接受率為44.4%。會議中安排有四場專業演講，四場主題演講，會議內容共有36個時段之論文發表分別於6/10至6/12舉行。6/10日至6/12日參加各場次之論文發表會，筆者於研討會會中發表兩篇論文:

1. Soft Switching Hybrid Converter with Low Circulating Current
2. Novel Parallel ZVS Converters with Shared Power Switches for Medium Power Applications

筆者論文中發表兩種不同方法之高效率高壓直流轉換器架構,此電路對實現高效率及低損耗的電源供應器有深入討論，此兩種電路架構都具有零電壓切換技術，文章中利用硬體電路實現結果來證明所提新型電力轉換器之實用性與優越性能，此兩篇文章獲得與會日本與歐洲學者之興趣，有熱烈討論與互相交流。該會議為一有關之工業電子應用之 IEEE 電力電子與電動機驅動國際研討會,會議內容包含電力電子技術、馬達製造、能源控制、智慧控制、混合式電動車之研究趨勢與再生能源應用。

三、 心得

IEEE-PEDS 電力電子與電動機驅動國際研討會為全世界有關電力電子及驅動系統相關研究方面重要會議之一。本次會議共有 200 篇論文。台灣有很多師生參與，包括交通大學電機系鄒應嶼教授，台北科技大學電機系劉邦榮教授及國內私立大學其他教授等共十多位人員參加。為提高台灣之學術地位及能見度，仍需國科會教育部繼續支持。在本次的會議中可以看出論文廣度加大，在會議中能認識其他國家的人士，彼此能交換心得，對於開拓視野、提升研究品質有莫大的幫助。會中與各國專家學者交換意見，獲益良多。茲將出席本次會議心得分述如下：

1．台灣學者在研究深度上與各國相比較，表現很好。
2．會中與各國專家學者交換高效率電源轉換器與再生能源技術，獲益良多。
3．與中國、日本及韓國學者在大會上廣泛互動與討論研究方向，作為將來合作之機會。
4．此次會議中較多研究論文發表集中再生能源發電系統，利用高效能轉換器技術讓整體電源技術之效率提升，利用智慧型控制理論，增加實用性之產品應用。
5.雲端電源技術之發展，在此次研討會中也是被討論主題之一。
6.大型高瓦數電動機控制系統在研討會中也受到相當之重視。

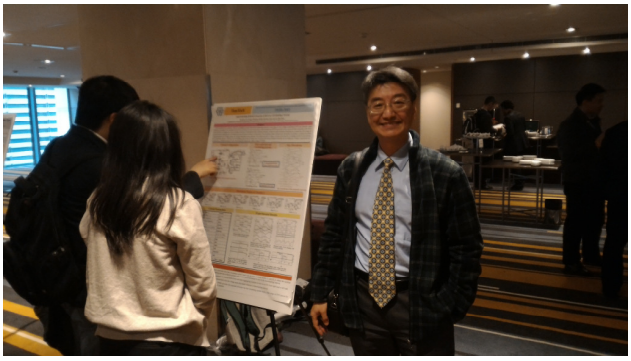
四、 建議事項

IEEE-PEDS 電力電子與電動機驅動國際研討會為 IEEE 有關電機電子相關研究方面重要的國際會議，所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對工業升級及發展高科技所需的高效率電源及驅動系統之發展，均有相當的影響。由於參與類似的學術性會議非常重要，故有以下建議:

1．鼓勵學者積極參與國際學術會議。
2．政府應對此領域之研究多作投資。
3.中國學者出席國際研討會近幾年相當積極，人數超出台灣學者很多，台灣在此方面要多鼓勵國內學者出席介紹台灣教學研究成果。

五、 附錄

發表論文資料。



論文發表現場

IEEE PEDS 2015, Sydney, Australia
9 – 12 June 2015

Soft Switching Hybrid Converter with Low Circulating Current

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***Abstract*–In this paper, a new hybrid dc-dc converter with low circulating current within the freewheeling interval, wide range of zero voltage switching (ZVS) and reduced output inductors is presented. The proposed hybrid circuit includes two three-level pulse-width modulation (PMW) converters and a series resonant converter with shard power switches in lagging leg. Series resonant converter is operated at fixed switching frequency (close to series resonant frequency) to extend the ZVS range of power switches at lagging leg. The output of series resonant converter is connected to the secondary sides of three-level converters to produce a positive rectified voltage instead of zero voltage. Hence, the output inductance can be reduced. The reflected positive voltage is used to decrease the circulating current to zero during the freewheeling interval. Therefore, the circulating current losses in three-level converters and series resonant converter are all improved. Finally, experiments are presented for a 1.44kW prototype circuit converting 800V input to an output voltage 24V/60A.**

I. Introduction

Modern medium dc power supplies based on three-level dc-dc converters has been developed to have the functions of low voltage stress of the switches, compact size and high circuit efficiency for industry and traction applications [1]-[2]. The main advantage of three-level dc-dc converters [3]-[5] is that zero voltage switching (ZVS) of all switches can be achieved. However, the main drawbacks of conventional three-level ZVS converters are high circulating current losses during the freewheeling interval and narrow range of ZVS at lagging-leg switches. The high circulating current increases conduction losses on switches and transformer windings and decreases circuit efficiency. In order to overcome these disadvantages, active or passive circuits can be added on the primary side or the secondary side [6]-[7] to reduce the voltage oscillation on the rectifier diodes and decrease the circulating current losses. However, the duty cycle loss is also increased that will decrease the effective duty cycle on the secondary side and the power losses of additional auxiliary circuits are also increased. Resonant converter and full-bridge converter with the shared active switches have been presented in [8]-[9] to extend ZVS range of power switches at lagging leg from zero to full load.

A hybrid soft switching dc-dc converter including two three-level PWM converters and a *LLC* converter is presented. The main advantages of the proposed converter are low circulating current loss during the freewheeling interval, wide ZVS load range at lagging-leg switches and low output filter inductances. The output sides of three-level PWM converters and *LLC* converter are connected in parallel. If the primary side voltages of three-level converters are positive or negative, energy is transferred from input voltage to output load through three-level converters. If three-level converters are operated at freewheeling interval, then energy is transferred from input voltage to output load through *LLC* converter. Hence, three-level converters and *LLC* converter transfer energy from input voltage to output load within the whole switching cycle. The positive rectified voltage instead of zero can be generated at the secondary side using the clamp diodes. Thus, the output filter current ripple can be reduced. The positive rectified voltage is reflected to the primary side of three-level converter to reduce the circulating current to zero during the freewheeling interval. Half-bridge *LLC* converter with split capacitors shares the same lagging-leg switches of conventional three-level PWM converter. The adopted series resonant frequency of *LLC* converter is close to switching frequency. Therefore, the ZVS operation of the lagging-leg switches from zero to full load and low circulating current losses on the primary side are achieved. Finally, experiments with a 1.44kW laboratory prototype converting 800V to 24V/60A are provided to verify the theoretical analysis and demonstrate the circuit performance.

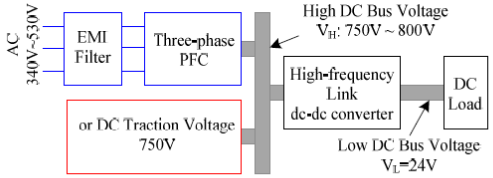

Fig. 1. System diagram of medium power three-phase ac-dc converter or dc traction power converter.

II. Circuit Configuration

Fig. 1 shows the circuit diagram of the medium power dc-dc converter used in three-phase ac/dc conversion or dc traction system applications. In three-phase ac-dc converter, three-phase PFC stage is operated to have high power factor, low current harmonics and high dc bus voltage. The high frequency link dc-dc converter converts high dc bus voltage V_H to low output voltage V_L. The circuit diagram of the proposed high frequency link dc-dc converter is shown in Fig. 2. The proposed circuit includes two three-level PWM converters and a *LLC* converter with a fixed switching frequency. Two three-level circuits are (C_{d1}, C_{d2}, D_a, D_b, C_{r1}, C_{r2}, S_1-S_4, C_1, L_{r1}, T_1, D_1, D_2 and L_{o1}) and (C_{d1}, C_{d2}, D_a, D_b,

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C_{r1}, C_{r2}, S_1-S_4, C_2, L_{r2}, T_2, D_3, D_4 and L_{o2}). *LLC* converter includes C_{r1}, C_{r2}, S_2, S_3, L_{r3}, T_3, D_5, D_6, D_c, D_d and C_{LLC}. Phase-shift pulse-width modulation is adopted to generate four gate voltages and to regulate output voltage against input voltage and load current variations. There are three voltage levels on v_{ab} and v_{bc}. *LLC* circuit is operated at the fixed switching frequency and fixed duty cycle. Hence, the output voltage of *LLC* converter v_{LLC} is an unregulated output voltage. The operated switching frequency f_{sw} is higher than the series resonant frequency f_r in *LLC* converter so that the lagging-leg switches S_2 and S_3 can be turned on at ZVS from light load to full load. The drawback of narrow load range of the lagging-leg switches in conventional three-level converter is overcome. The clamp diodes D_c and D_d are connected between the *LLC* output C_{LLC} and the rectified points *d* and *e* of two three-level converters. Clamp diodes D_c and D_d are conducting during the freewheeling interval to transfer energy from *LLC* output v_{LLC} to three-level converter output V_o. At this moment, the rectified voltages $v_{rect,1}$ and $v_{rect,2}$ are equal to v_{LLC}. The reflected voltages $n_{T1}v_{rect,1}$ and $n_{T2}v_{rect,2}$ are applied to L_{r1} and L_{r2}, respectively, to decrease the primary side currents i_{Lr1} and i_{Lr2} to zero during the freewheeling interval. Therefore, the high circulating losses problem in conventional three-level dc-dc converter is overcome in the proposed converter. The voltage across output inductors v_{Lo1}=v_{Lo2}=v_{LLC}-V_o instead of -V_o in the freewheeling interval so that the output inductor current ripple can be reduced for the proposed converter and the output inductances L_{o1} and L_{o2} can be reduced at the given output current ripple condition.

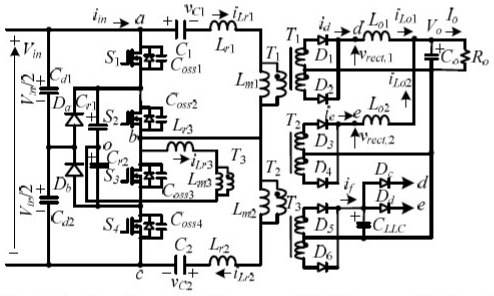


Fig. 2. Circuit configuration of the proposed high frequency link three-level ZVS converter.

III. Operation Principles

The duty cycle of power switches S_1-S_4 equals 0.5 with the fixed switching frequency f_{sw}. Phase-shift PWM scheme is adopted to generate gate voltages of S_1-S_4. The gating signal of S_2 (S_3) is phase-shifted with respective to the gating signal of S_1 (S_4). S_1 and S_4 are in the leading-leg and S_2 and S_3 are in the lagging-leg. S_1 (S_2) and S_4 (S_3) operate complementarily with a short dead time to avoid short circuit at high voltage side. Before the discussions of the operation principles, some assumptions are made to simplify the system analysis. Switches S_1-S_4 and rectifier diodes D_a-D_d and D_1-D_6 are ideal. Turns ratios of T_1-T_3 are n_1=n_2=n_{p1}/n_{s1}=n_{p1}/n_{s2} and n_3=n_{p3}/n_{s5}=n_{p3}/n_{s6}. C_1=C_2=C_c and C_{oss1}=..=C_{oss4}=C_{oss}. V_{Cd1}=V_{Cd2}=V_{Cr1}+V_{Cr2}=V_{in}/2. L_{r1}=L_{r2}=L_r and L_{o1}=L_{o2}=L_o. The key waveforms for different operation modes are shown in Fig. 3. Based on the on/off states of S_1-S_4, D_a-D_d, and D_1-D_6, there are six switching modes during each half switching cycle. The equivalent circuits for different operation modes are given in Fig. 4.

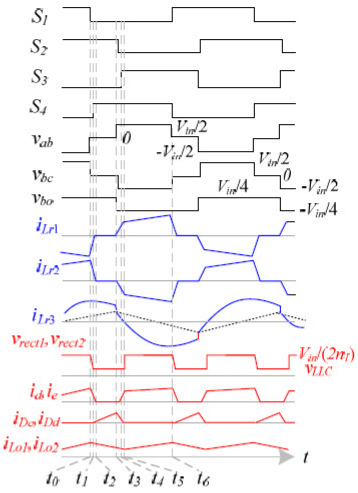


Fig. 3. Key waveforms of the proposed converter during the first half switching cycle.

Mode 1 [t_0 - t_1]: Prior to t_0, power semiconductors S_1, S_2, D_2, D_3 and D_5 are conducting. i_{Lr1} decreases and i_{Lr2} and i_{Lr3} increase. At time t_0, S_1 is turned off. The primary side currents i_{Lr1} and i_{Lr2} start to charge and discharge the output capacitors C_{oss1} and C_{oss4}, respectively. The energy stored in output inductors L_{o1} and L_{o2} is reflected to the primary side to discharge C_{oss4}. Thus, the ZVS condition of S_4 is easily achieved and given as

$$(L_{r1}+n_1^2L_o)i_{Lr1}^2(t_0)+(L_{r2}+n_2^2L_o)i_{Lr2}^2(t_0)\geq\frac{C_{oss}V_{in}^2}{2} \quad (1)$$

Mode 1 ends at time t_1 when v_{Coss1}=V_{in}/2 and v_{Coss4}=0. The duration of this period is expressed in (2).

$$\Delta t_{01}=t_1-t_0=\frac{C_{oss}V_{in}}{i_{Lr1}(t_0)+i_{Lr2}(t_0)}\approx\frac{C_{oss}V_{in}}{i_{Lo1,\max}/n_1+i_{Lo2,\max}/n_2} \quad (2)$$

After the dead time (t_{dead}>Δt_{01}), S_4 is turned on at ZVS.

Mode 2 [t_1 - t_2]: At time t_1, drain-source voltage of S_4 (v_{Coss4}) reaches to zero. The primary current i_{Lr2} flows through the body diode of S_4 so that S_4 can be turned on at this moment under ZVS. Since the output voltage of *LLC* converter v_{LLC} is greater than the secondary winding voltage of T_1 and T_2, diodes D_c and D_d are forward biased. The rectified voltages $v_{rect,1}$and $v_{rect,2}$ are both equal to v_{LLC}. The output inductor voltages v_{Lo1}=v_{Lo2}=v_{LLC}-V_o<0. Hence, i_{Lo1} and i_{Lo2} decrease during this interval. The ac terminal voltages at primary side v_{ab}=v_{bc}=V_{in}/2 and V_{C1}=V_{C2}=V_{in}/2, and the reflected secondary windings voltages n_1v_{LLC} and -n_2v_{LLC} are applied to L_{r1} and L_{r2}, respectively. The primary currents i_{Lr1} and i_{Lr2} are rapidly reset to zero. The duration of this period is derived as

$$\Delta t_{12} = t_2 - t_1 = \frac{L_{r1} i_{Lo1}(t_2)/n_1}{n_1 v_{LLC}} \approx \frac{L_{r1} i_{Lo1,\max}}{n_1^2 v_{LLC}} \quad (3)$$

In conventional three-level dc-dc converter, the primary currents i_{Lr1} and i_{Lr2} are almost keeping at the same current value as $i_{Lr1}(t_1)$ and $i_{Lr2}(t_2)$ because $v_{Lr1}=v_{Lr2}=0$. Thus, the conventional three-level dc-dc converter has large circulating current losses during the freewheeling interval. The large circulating current will result in more conduction losses. In this mode, the energy stored in C_{LLC} is transferred to output load through D_c, D_d, L_{o1} and L_{o2}, the secondary side currents i_d and i_e decrease, and diode currents i_{Dc} and i_{Dd} increase. *LLC* circuit is operated at resonant mode to transfer energy from input voltage to output capacitor C_{LLC}.

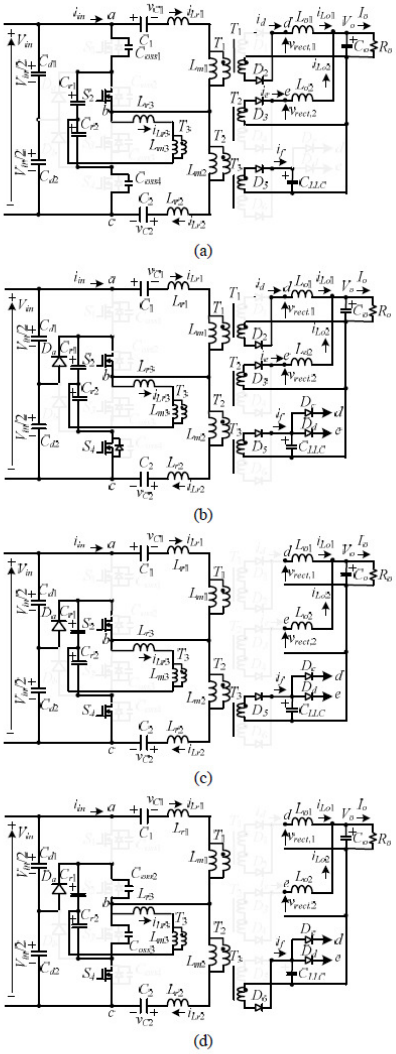


Fig. 4. Operation modes of the proposed converter in a half switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6.

Mode 3 [t_2 - t_3]: At time t_2, the secondary side currents of transformers T_1 and T_2 are decreased to zero. The primary and secondary sides of T_1 and T_2 are disconnected and the rectifier diodes D_1-D_4 are all reverse biased. *LLC* converter continuous to transfer energy from input source to output load with $i_{Dc}=i_{Lo1}$ and $i_{Dd}=i_{Lo2}$.

Mode 4 [t_3 - t_4]: At time t_3, S_2 is turned off. The primary side currents i_{Lr1}, i_{Lr2} and i_{Lr3} start to charge C_{oss2} and discharge C_{oss3}. Since *LLC* converter is operated at inductive load ($f_{sw}>f_r$), the primary current i_{Lr3} is lagging to input fundamental voltage. Hence, lagging-leg switch S_3 can be easily turned on under ZVS at t_4 from light load to full load.

Mode 5 [t_4 - t_5]: At time t_4, the drain-source voltage of S_3 (v_{Coss3}) reaches to zero. Since $i_{Lr3}(t_4)>0$, the body diode of S_3 is conducting and S_3 can be turned on at this moment at ZVS. The ac terminal voltages $v_{ab}=V_{in}$ and $v_{bc}=0$. However, the clamp diodes D_c and D_d are still conducting in this mode to transfer energy from C_{LLC} to output load. The rectified voltages $v_{rect,1}=v_{rect,2}=v_{LLC}$ and inductor voltage $v_{Lo1}=v_{Lo2}=v_{LLC}-V_o<0$. The output inductor currents i_{Lo1} and i_{Lo2} decrease in this mode. *LLC* converter is resonant with negative input voltage $-v_{Cr2}$. Thus, i_{Lr3} decreases in this mode. The clamp diode currents i_{Dc} and i_{Dd} are decreased. Both three-level dc-dc converter and *LLC* converter transfer energy from input side to output load during this interval. The primary side inductor voltages $v_{Lr1}=V_{in}/2-n_1 v_{LLC}>0$ and $v_{Lr2}=n_2 v_{LLC}-V_{in}/2<0$. Therefore, i_{Lr1} increases and i_{Lr2} decreases, respectively, until i_{Lr1} equals i_{Lo1}/n_1 and i_{Lr2} equals $-i_{Lo2}/n_2$. Then D_c and D_d are turned off. The duration of this period is given as

$$\Delta t_{45} = t_5 - t_4 = \frac{L_{r1} i_{Lo1}(t_5)/n_1}{V_{in}/2 - n_1 v_{LLC}} \approx \frac{2 L_{r1} i_{Lo1,\min}}{n_1 (V_{in} - 2 n_1 v_{LLC})} \quad (4)$$

Mode 6 [t_5 - t_6]: At time t_5, diode currents i_{Dc}=i_{Dd}=0, i_d=i_{Lo1} and i_e=i_{Lo2}. Then, diodes D_c and D_d are turned off. The energy is transferred from input voltage to output load through three-level dc-dc converter. The output inductor voltages v_{Lo1}=V_{in}/(2n_1)-V_o>0 and v_{Lo2}=V_{in}/(2n_2)-V_o>0. Both inductor currents i_{Lo1} and i_{Lo2} increase in this mode. This mode ends at time t_6 when S_4 is turned off. Then, the circuit operations of the proposed converter in a half switching cycle are completed.

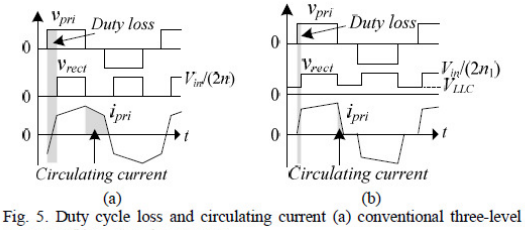


Fig. 5. Duty cycle loss and circulating current (a) conventional three-level converter (b) proposed converter.

IV. Circuit Characteristics

The features of the proposed converter are low duty cycle loss, low circulating current, low output inductance and more effective energy transfer. The duty cycle loss and the primary circulating current of the conventional three-level dc-dc converter and the proposed converter are shown in Fig. 5. It can be seen that there is a large circulating current flowing through the transformer and power switches in the freewheeling interval (v_{pri}=0). This circulating current results in high conduction losses at the primary side especially at full load and low duty cycle conditions. However, this drawback is improved in the proposed converter. During the freewheeling interval, a positive rectified voltage instead of zero voltage at the secondary side is reflected to the primary side to rapidly reduce the primary current to zero. Hence, the primary circulating current in the proposed converter is minimized. In order to extend the ZVS range of lagging-leg switches, the large value of leakage inductance or external series inductance is usually adopted in conventional three-level converter. However, the large leakage inductor or external series inductor will also increase the duty cycle losses due to the time requirement from negative to positive primary current or from positive to negative primary current. Thus, a lower turns ratio of transformer is needed to compensate the duty cycle loss. However, a lower turns ratio of transformer will result in the higher primary side current and higher voltage stress on the secondary side. Thus, the conduction losses at primary and secondary sides are also increased. In the freewheeling interval, the primary current in the proposed converter is increased from zero instead of negative current value to positive current value. Thus, the commutated time shown in (4) in the proposed converter is much less than that in conventional three-level converter. That means that a higher turns ratio of transformer can be used to reduce the primary side current and the voltage stress of rectifier diodes.

In conventional three-level converter, the output inductance is given as

$$\Delta i_{Lo} \approx \frac{V_o(0.5-\delta_{eff})T_{sw}}{L_o} = \frac{V_{in}\delta_{eff}(1-2\delta_{eff})T_{sw}}{2nL_o} \quad (5)$$

where δ_{eff} (<0.5) is an effective duty cycle and n is the turns ratio of isolation transformer between primary winding turns and secondary winding turns. In the proposed converter, energy is transferred from input voltage to output load through *LLC* converter in modes 2-5 and three-level converter in modes 1, 2, 5 and 6. Hence, energy is transferred from input voltage to output load within the full switching cycle. The *LLC* converter is operated as an unregulated dc-dc converter with the switching frequency close to series resonant frequency. Thus, the lagging-leg switches S_2 and S_3 are turned on at ZVS from zero to full load. The circulating current of the *LLC* circuit is also minimum due to f_{sw}≈f_r. The designed dc voltage gain of *LLC* converter equals the ac voltage gain of *LLC* converter at series resonant frequency, i.e. $M_{dc,LLC}$=4n_3V_{LLC}/V_{in}=1. The output average voltage of *LLC* converter can be derived as

$$V_{LLC} = V_{in}/(4n_3) \quad (6)$$

The ZVS turn-on condition of leading-leg switches S_1 and S_4 is achieved by the primary inductances L_{r1} and L_{r2} and the output inductances L_{o1} and L_{o2}, given in (1). Since the charge and discharge time of S_1-S_4 are negligibly small compared to the other time intervals, only modes 2, 3, 5 and 6 are considered in the first half switching period in order to obtain the output voltage of the proposed converter. Apply the flux balance to (L_{r1} and L_{m1}) and (L_{r2} and L_{m2}), the average capacitor voltages V_{C1} and V_{C2} are obtained as

$$V_{C1} = V_{C2} = V_{in}/2 \quad (7)$$

In mode 5, the ac terminal voltages v_{ab}=V_{in} and v_{bc}=0. However, diodes D_c and D_d are conducting in this mode. The rectified voltages $v_{rect,1}$=$v_{rect,2}$=v_{LLC}. The duty cycle loss in mode 5 can be obtained as

$$\delta_5 = \Delta t_{45}/T_s \approx \frac{2L_{r1}I_{Lo1}f_{sw}}{n_1(V_{in}-2n_1v_{LLC})} = \frac{4L_{r1}I_{Lo1}f_{sw}}{n_1V_{in}(2-n_1/n_3)} \quad (8)$$

The effective duty cycle in the primary side is given as δ_{eff}=δ-δ_5. δ is the duty ratio of the proposed converter when (S_1 and S_2) or (S_3 and S_4) are in the on-state. Based on the flux balance on output inductors L_{o1} and L_{o2}, the output voltage V_o of the proposed hybrid converter is derived as:

$$V_o = \delta_{eff}V_{in}/n_1 + (1-2\delta_{eff})V_{LLC} = (\frac{1}{4n_3} + \frac{\delta_{eff}}{n_1} - \frac{\delta_{eff}}{2n_3})V_{in} \quad (9)$$

From (9), the voltage conversion ratio is given as

$$M_{DC} = \frac{V_o}{V_{in}} = \frac{1}{4n_3} + \frac{\delta_{eff}}{n_1} - \frac{\delta_{eff}}{2n_3} \quad (10)$$

In steady state, the average output inductor currents are assumed balanced, I_{Lo1}=I_{Lo2}=I_o/2. The ripple currents of L_{o1} and L_{o2} are approximately derived as

$$\Delta i_{Lo1} = \Delta i_{Lo2} \approx \frac{(V_o - V_{LLC})(0.5-\delta_{eff})T_{sw}}{L_o} \quad (11)$$

Substituting (6) and (10) into (11) yields

$$\Delta i_{Lo1} = \Delta i_{Lo2} = \frac{V_{in}\delta_{eff}(1-2\delta_{eff})(\frac{1}{n_1}-\frac{1}{2n_3})T_{sw}}{2L_o} \quad (12)$$

Compared to the conventional three-level converter, the proposed converter has less inductor current ripple. It means that the output inductances L_{o1} and L_{o2} in the proposed converter can be reduced at the given inductor current ripple case. Hence, the core size and copper loss of the output inductors are also reduced in the proposed converter. If the defined ripple currents Δi_{Lo1} and Δi_{Lo2} are given, then the output inductances L_{o1} and L_{o2} can be obtained from (12). Based on the charge balance on C_1, C_2, C_{r1} and C_{r2}, one obtains the average magnetizing currents $I_{Lm1}=I_{Lm2}=I_{Lm3}=0$. The ripple currents of L_{m1}-L_{m3} are derived as

$$\Delta i_{Lm1} = \Delta i_{Lm2} \approx V_{in}\delta_{eff}T_{sw}/(2L_{m1}) \quad (13)$$

$$\Delta i_{Lm3} \approx V_{in}T_{sw}/(8L_{m3}) \quad (14)$$

Based on (13) and (14), the maximum and minimum magnetizing currents of T_1-T_3 are given as:

$$i_{Lm1,\max} = i_{Lm2,\max} = V_{in}\delta_{eff}T_{sw}/(4L_{m1}) \quad (15)$$

$$i_{Lm1,\min} = i_{Lm2,\min} = -V_{in}\delta_{eff}T_{sw}/(4L_{m1}) \quad (16)$$

$$i_{Lm3,\max} = V_{in}T_{sw}/(16L_{m3}),\ i_{Lm3,\min} = -V_{in}T_{sw}/(16L_{m3}) \quad (17)$$

The average diode currents and voltage stresses of D_1-D_6, D_c and D_d in steady state are expressed as:

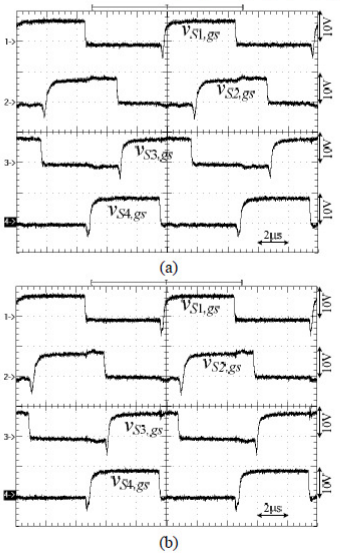
$$i_{D1,\text{av}} = i_{D2,av} = i_{D3,\text{av}} = i_{D4,av} \approx \delta I_o/2 \quad (18)$$

$$i_{D5,\text{av}} = i_{D6,av} = i_{Dc,\text{av}} = i_{Dd,av} \approx (0.5-\delta)I_o/2 \quad (19)$$

$$v_{D1,\text{stress}} = v_{D2,\text{stress}} = v_{D3,\text{stress}} = v_{D4,\text{stress}} \approx V_{in}/n_1 \quad (20)$$

$$v_{D5,\text{stress}} = v_{D6,\text{stress}} \approx 2V_{LLC} = V_{in}/(2n_3) \quad (21)$$

$$v_{Dc,\text{stress}} = v_{Dd,\text{stress}} \approx V_{in}/(2n_1) - V_{LLC} = (2n_3 - n_1)V_{in}/(4n_1n_3) \quad (22)$$



(a)

(b)

Fig. 6. Measured results of the gate voltages of S_1-S_4 (a) V_{in}=800V and 50% load (b) V_{in}=800V and 100% load.

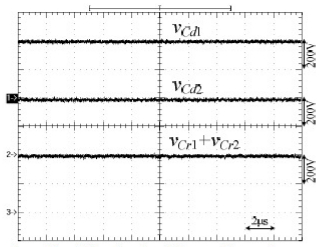


Fig. 7. Measured results of the input split capacitor voltages v_{Cd1} and v_{Cd2} and the resonant capacitor voltages $v_{Cr1}+v_{Cr2}$ at V_{in}=800V and full load.

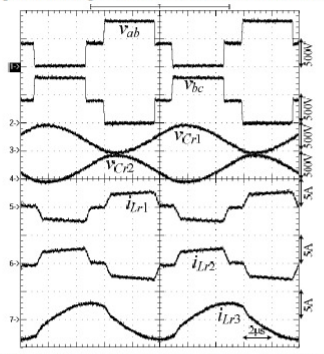


Fig. 8. Measured results of the ac side voltages, the resonant capacitor voltages and primary side currents at V_{in}=800V and full load.

V. Experimental Results

Experimental results of a laboratory prototype are provided in this section to demonstrate the performance of the proposed converter. The specifications of the proposed converter are V_{in}=750V-800V, V_o=24V, $I_{o,rated}$=60A, f_{sw}=100kHz. First, the output voltage of *LLC* converter is assumed as 20V. The resonant frequency of *LLC* converter is designed at $f_r \approx f_{sw}$. Thus, the circulating current of *LLC* converter is less than the circulating current of the converter operated at $f_{sw}<f_r$. The DC gain of LLC converter at f_r is equal to unity. The turns ratio of T_3 is 10. The assumed maximum effective duty cycle δ_{eff} is 0.4. The primary and secondary winding turns of T_1 and T_2 are selected as 74 turns and 5 turns, respectively. The magnetizing inductances of T_1 and T_2 are 3mH. The necessary primary inductances $L_{r1}=L_{r2}$=24μH. In *LLC* converter, the series resonant inductance L_{r3}=120μH and resonant capacitances $C_{r1}=C_{r2}$=11μF. The primary inductance, primary winding turns and secondary winding turns of T_3 are 600μH, 60 turns and 6 turns, respectively. The allowed ripple current on L_{o1} and L_{o2} is about 2% of rated load current. The output inductances L_{o1} and L_{o2} are 12μH. The MOSFETs IRFP460 with V_{DS}=500V, $I_{D,rms}$=20A, $R_{DS,on}$=0.27Ω and C_{oss}=480pF at 25V are used for switches S_1-S_4. Fast recovery diodes SBR40U100 with V_{RRM}=100V and I_F=40A are used as the rectifier diodes D_1-D_6, D_c and D_d. The selected clamped

diodes D_a and D_b are RHRP3060. The selected input split capacitances are C_{d1}=C_{d2}=220μF/450V, dc blocking capacitances C_1=C_2=20μF and the output capacitances are C_{LLC}=50μF and C_o=6600μF. Phase-shift PWM IC UC3895 is adopted to achieve the load voltage regulation and PWM generation of S_1-S_4. Experimental results are provided to verify the operation principles and performance of the proposed converter. The experimental results of the gate voltages of S_1-S_4 at 50% load 100% load with 800V input are shown in Fig. 6. Fig. 7 shows the measured waveforms of the input spilt capacitor voltages v_{Cd1} and v_{Cd2} and the resonant capacitor voltages v_{Cr1}+v_{Cr2} at full load. It can be seen that these three voltages are balanced. Fig. 8 illustrates the experimental results of the ac side voltages v_{ab} and v_{bc}, resonant capacitor voltages v_{Cr1} and v_{Cr2} and the primary side currents i_{Lr1}-i_{Lr3} at full load. It is clear that there are three voltage levels on v_{ab} and v_{bc}. The primary currents i_{Lr1} and i_{Lr2} decrease to zero during the freewheeling interval. Therefore, the circulating current losses are improved in the proposed converter. Fig. 9 gives the measured results of the gate voltages, drain voltages and drain currents of S_1 (leading-leg switch) and S_2 (lagging-leg switch) at different load conditions. It can be seen that S_1 (leading-leg switch) can be turned on at ZVS from 25% load and S_2 (lagging-leg switch) can be turned on at ZVS from 17% load. Fig. 10 shows the test results of the secondary side currents at 100% load. When the ac side voltage v_{ab}=V_{in} and 0, three-level converters transfer energy from input voltage to output load (i_d>0 and i_e>0). On the other hand, *LLC* circuit transfers energy from C_{r1} and C_{r2} to output load (i_{Dc}>0 and i_{Dd}>0) when the ac side voltage v_{ab}=V_{in}/2.

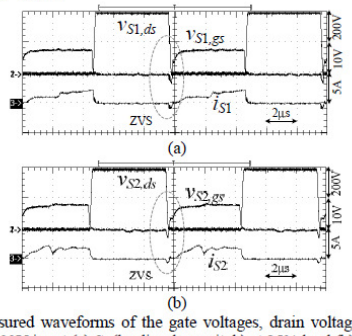


Fig. 9. Measured waveforms of the gate voltages, drain voltages and drain currents at 800V input (a) S_1 (leading-leg switch) at 25% load (b) S_2 (lagging-leg switch) at 17% load.

VI. Conclusion

A new ZVS dc-dc converter is presented in this paper. The proposed converter includes two three-level PWM converters and a *LLC* converter. In the proposed converter, three-level converters have less circulating current losses with the help of clamp diodes D_c and D_d to obtain the rectified voltages $v_{rect,1}$=$v_{rect,2}$=V_{LLC} in freewheeling intervals so that the primary side currents can be decreased to zero in the freewheeling interval. *LLC* converter operates at f_{sw}≈f_r with minimum circulating current losses and helps lagging-leg switches to turn on at ZVS from light load to full load. The energy is transferred from input to output load within the whole switching cycle. Hence, the proposed converter has more effective energy transfer. The output inductances L_{o1} and L_{o2} are reduced due to the less voltage across the output inductors in freewheeling interval. Compared to the conventional three-level PWM converter, the proposed converter has less circulating current losses, wide range of ZVS turn-on for lagging-leg switches and the reduced output inductors. Finally, experiments with a 1440W prototype circuit are provided to verify the performance of the proposed converter.

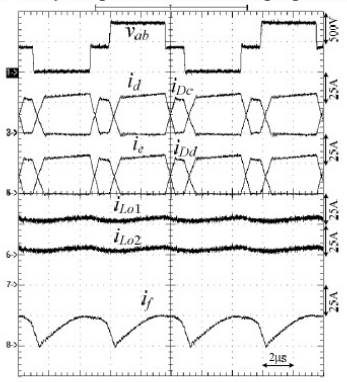


Fig. 10. Measured results of the secondary side currents at full load.

Acknowledgment

This project is supported by the National Science Council of Taiwan under Grant NSC102-2221-E-224-022-MY3.

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IEEE PEDS 2015, Sydney, Australia
9 – 12 June 2015

Novel Parallel ZVS Converters with Shared Power Switches for Medium Power Applications

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Abstract- **A new DC/DC converter with parallel circuits is presented for medium voltage and power applications. There are five pulse-width modulation (PWM) circuits in the proposed converter to reduce current stress at low voltage side for high output current. These five circuits have the same power switches so that the switch counts are reduced compared with the conventional parallel converters. In order to reduce the converter size, conduction loss and voltage stress of power semiconductors, the series connections of power MOSFETs with high switching frequency instead of IGBTs with low switching frequency are adopted. Thus, the voltage stress of MOSFETs is clamped at half of input voltage. The switched capacitor circuit is adopted to balance input split capacitor voltages. Asymmetric PWM scheme is adopted to generate the necessary switching signals of MOSFETs and regulate output voltage. Based on the resonant behavior at the transition interval of power switches, all MOSFETs are turned on under zero voltage switching (ZVS) from 50% load to 100% load. The circuit configuration, operation principle, converter performance and design example are discussed in detail. Finally, experimental verifications with a 1.92kW prototype are provided to verify the performance of the proposed converter.**

I. Introduction

Modern switching converters for medium input voltage [1]–[2] have been developed for DC traction system, rapid transit systems or medium power applications with three-phase AC input. Multilevel converters [3]-[6] have developed to lessen voltage stress of power devices and increase the switching frequency so that the converter size can be reduced. However, power devices in these topologies are operated at hard switching and the switching losses are increased if the high switching frequency is adopted. Therefore, soft switching techniques were proposed for multilevel converters [7]-[15] to improve circuit efficiency. In [7]-[11], the auxiliary circuits are adopted in three-level converter with asymmetric or phase-shift pulse-width modulation (PWM) to achieve zero voltage switching (ZVS) or zero current switching (ZCS) for power switching or extent the ZVS load range. In [14], three-level converters with resonant circuit were developed to have zero voltage switching (ZVS) on power devices and zero current switching (ZCS) on rectifier diodes. The variable switching frequency is adopted to control DC voltage gain and regulate output voltage. The ripple current at output capacitor is much larger than that of the conventional three-level converter. Three-level resonant converters with duty cycle control were presented in [15] to have soft switching on power devices with fixed switching frequency. However, these control schemes have high circuit efficiency if the duty cycle is close to half of switching period. If the input voltage is increased, then the duty cycle is decreased and the conduction losses are increased. Thus, the converter cannot be maintained at high circuit efficiency at different loads or input voltage cases. For medium voltage and load current applications, parallel three-level converters are needed if the high load usually adopted to distribute the load power into several sub-circuits with low current rating of power semiconductors and passive components. However, parallel topologies normally need several control units to individually control each sub-circuit. Hence, there are too many power switches and control units in conventional parallel converters.

A new soft switching PWM DC/DC converter is presented in this paper to achieve the functions of 1) less switch counts compared with the conventional parallel three-level DC/DC converters, 2) ZVS turn-on for all power switches, 3) small size, light weight and low current stress of passive components, 4) low voltage stress of power switches, and 5) the balanced input split capacitor voltages. In order to reduce the component size to meet the compact size demands for medium power applications, the high frequency link DC/DC converter with parallel topology is used in the proposed converter. The proposed converter includes five DC/DC sub-circuits with shared power switches to distribute the total power into each sub-circuit. Hence, total switch counts are reduced compared with the conventional parallel converters and each circuit only have one-fifth of total power rating. Asymmetric PWM scheme is adopted to generate the properly gating signals of all power switches to achieve ZVS operation. Finally, experiments are presented for a 1.92*k*W prototype circuit converting 800V input to an output voltage 24V/80A for industry power supplies or battery chargers.

II. Circuit Configuration

For medium input voltage applications such as DC traction systems or three-phase AC/DC converters, input voltage of DC/DC converters will be higher than 750V. Thus, the voltage stress of power switches should be greater than 800V. Power MOSFETs with high voltage stress have large turn-on resistance and the conduction loss on MOSFETs is increased. To solve this problem, the series half-bridge circuits are proposed in Fig. 1. The voltage stress of MOSFETs is clamped at $V_{in}/2$ so that MOSFETs with 600V voltage stress can be used in the proposed converter for 750V input applications. The circuit components at high voltage side have input voltage V_{in}, input split capacitors C_1-C_4, power MOSFETs S_1-S_4 with their body diodes and parallel capacitors C_{r1}-C_{r4}, DC blocking capacitors C_5-C_8, resonant inductors L_{r1}-L_{r5}, and transformers T_1-T_5. At low voltage and

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high current side, five center-tapped rectifiers are connected in parallel to reduce the current stress of transformer windings, rectifier diodes D_1-D_{10} and output filter inductors L_{o1}-L_{o5}. Five ZVS circuits are adopted in the proposed converter to share load current. Circuits 1, 2 and 4 are based on the half-bridge topology with split capacitors. Circuits 3 and 5 are based on half-bridge topology with transformer connected to high voltage side and ground point, respectively. Power MOSFETs S_1 and S_3 have same PWM waveforms with duty cycle δ. However, MOSFETs S_2 and S_4 have same PWM waveforms with duty cycle (1-δ). The components S_1-S_4, C_1-C_4, C_6 and C_7 establish a switched capacitor circuit [16]. Therefore, input split capacitor voltages are balanced, $v_{C1}+v_{C2}=v_{C3}+v_{C4}=v_{C6}+v_{C7}=V_{in}/2$. Asymmetric PWM is used to generate PWM signals S_1-S_4 and regulate output voltage at the desired voltage level.

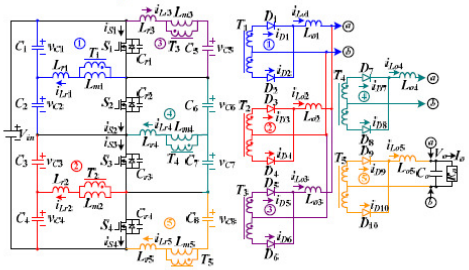


Fig. 1. Circuit configuration of the proposed ZVS converter with medium input voltage.

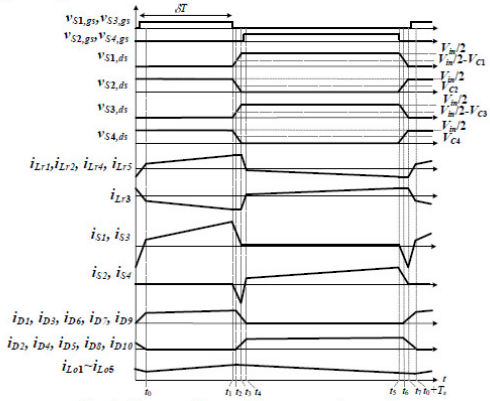


Fig. 2. Key waveforms of the proposed converter.

III. Operation Principles

In the proposed converter, asymmetric PWM scheme is used to control output voltage. The following assumptions are presumed to simplify the circuit analysis. Transformers T_1-T_5 have the same magnetizing inductances L_m and same turns ratio $n=n_p/n_{s1}=n_p/n_{s2}$. S_1-S_4 have the same output capacitances $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$. Voltage $v_{C1}+v_{C2}=v_{C3}+v_{C4}=V_{in}/2$. $C_5=C_8=2C_1=2C_2=2C_3=2C_4=2C_6=2C_7=C_c$. $L_{r1}=..=L_{r5}=L_r$ and $L_{o1}=L_{o2}=L_{o3}=L_{o4}=L_{o5}=L_o$. The main PWM waveforms of the proposed converter are given in Fig. 2. The corresponding equivalent circuits for each operation mode are shown in Fig. 3. Before time t_0, S_2 and S_4 are in the off-state and diodes D_1-D_{10} are all conducting.

***Mode 1* [t_0 - t_1]:** Mode 1 begins at t_0 when diode currents of D_2, D_4, D_5, D_8 and D_{10} are decreasing to zero. The voltage stresses of S_2 and S_4 are equal to $v_{C1}+v_{C2}$ and $v_{C3}+v_{C4}$, respectively. In this mode, $v_{C6}+v_{C7}=v_{C1}+v_{C2}$. However, $v_{C6}+v_{C7}=v_{C3}+v_{C4}$ in mode 5. It can be derived that $v_{C1}+v_{C2}=v_{C3}+v_{C4}=v_{C6}+v_{C7}=V_{in}/2$ in steady state. Thus, the voltage stresses of S_2 and S_4 are equal to $V_{dc}/2$. In this mode, the primary side currents i_{Lr1}, i_{Lr2}, i_{Lr4} and i_{Lr5} increase and i_{Lr3} decreases. Power is transferred from input voltage V_{in} to output load R_o in this mode.

***Mode 2* [t_1 - t_2]:** Mode 2 begins at time t_1 when S_1 and S_3 are turned off. In this mode, $i_{Lr1}(t_1)>0$, $i_{Lr2}(t_1)>0$, $i_{Lr3}(t_1)<0$, $i_{Lr4}(t_1)>0$ and $i_{Lr5}(t_1)>0$. Thus, C_{r1} and C_{r3} are charged and C_{r2} and C_{r4} are discharged rapidly so that i_{Lr1}-i_{Lr5} and i_{Lo1}-i_{Lo5} are almost constant in this mode.

***Mode 3* [t_2 - t_3]:** Mode 3 begins at t_2 when $v_{Cr1}=v_{C1}=v_{C5}$, $v_{Cr2}=v_{C2}=v_{C6}$, $v_{Cr3}=v_{C3}=v_{C7}$ and $v_{Cr4}=v_{C4}=v_{C8}$. The primary and secondary winding voltages of T_1-T_5 equal zero voltage. In this mode, D_1-D_{10} are conducting, i_{D1}, i_{D3}, i_{D6}, i_{D7} and i_{D9} decrease, and i_{D2}, i_{D4}, i_{D5}, i_{D8} and i_{D10} increase. The output inductor voltages $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=v_{Lo5}=-V_o$ and the inductor currents i_{Lo1}-i_{Lo5} all decrease. Since $i_{Lr1}(t_2)>0$, $i_{Lr2}(t_2)>0$, $i_{Lr3}(t_2)<0$, $i_{Lr4}(t_2)>0$ and $i_{Lr5}(t_2)>0$, C_{r1} and C_{r3} are continuously charged and C_{r2} and C_{r4} are continuously discharged. C_{r2} and C_{r4} can be discharged to zero voltage at t_3 if the energy stored in L_{r1}-L_{r5} is greater than the energy stored in C_{r1}-C_{r4}.

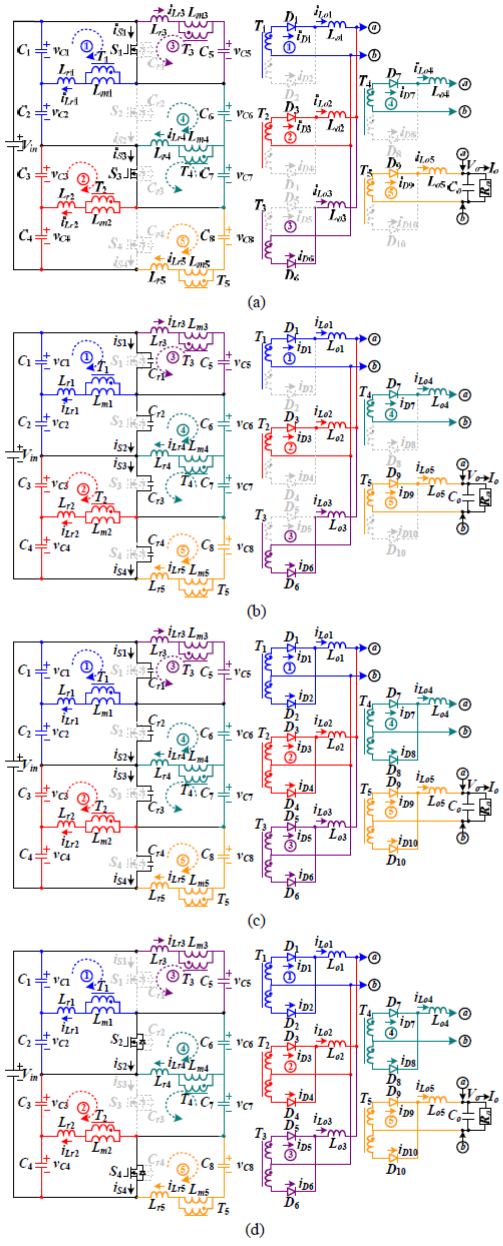
***Mode 4* [t_3 - t_4]:** Mode 4 begins at time t_3 when $v_{Cr2}=v_{Cr4}=0$, $v_{Cr1}=v_{C1}+v_{C2}$ and $v_{Cr3}=v_{C3}+v_{C4}$. Since $i_{Lr1}(t_3)>0$, $i_{Lr2}(t_3)>0$, $i_{Lr3}(t_3)<0$, $i_{Lr4}(t_3)>0$ and $i_{Lr5}(t_3)>0$, the anti-parallel diodes of S_2 and S_4 are conducting. Therefore, S_2 and S_4 can be turned on at this moment to achieve ZVS. In this mode, rectifier diodes D_1-D_{10} are still conducting. The inductor voltages $v_{Lr1}=-v_{C2}$, $v_{Lr2}=-v_{C4}$, $v_{Lr3}=v_{C1}+v_{C2}-v_{C5}$, $v_{Lr4}=-v_{C6}$, $v_{Lr5}=-v_{C8}$ and $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=v_{Lo5}=-V_o$. Therefore, i_{Lr3} increases, and i_{Lr1}, i_{Lr2}, i_{Lr4}, i_{Lr5} and i_{Lo1}-i_{Lo5} all decrease in this mode.

***Mode 5* [t_4 - t_5]:** Mode 5 begins at time t_4 when i_{D1}, i_{D3}, i_{D6}, i_{D7}, and i_{D9} are decreased to zero ampere. Thus, D_1, D_3, D_6, D_7, and D_9 are turned off. The voltage stresses of S_1 and S_3 are equal to $v_{C1}+v_{C2}$ and $v_{C3}+v_{C4}$, respectively. The voltage across C_6 and C_7 is equal to $v_{C3}+v_{C4}$. In this mode, the primary side currents i_{Lr1}, i_{Lr2}, i_{Lr4} and i_{Lr5} decrease and i_{Lr3} increases. Power is transferred from input voltage V_{in} to output load R_o in this mode.

***Mode 6* [t_5 - t_6]:** Mode 6 starts at time t_5 when S_2 and S_4 are turned off. Since $i_{Lr1}(t_5)<0$, $i_{Lr2}(t_5)<0$, $i_{Lr3}(t_5)>0$, $i_{Lr4}(t_5)<0$ and $i_{Lr5}(t_5)<0$, C_{r1} and C_{r3} are discharged and C_{r2} and C_{r4} are charged linearly so that all inductor currents are almost constant in this time interval.

***Mode 7* [t_6 - t_7]:** Mode 7 starts at time t_6 when $v_{Cr1}=v_{C1}=v_{C5}$, $v_{Cr2}=v_{C2}=v_{C6}$, $v_{Cr3}=v_{C3}=v_{C7}$ and $v_{Cr4}=v_{C4}=v_{C8}$. Thus, the secondary voltages of T_1-T_5 are equal to zero voltage so that diodes D_1-D_{10} are conducting, i_{D1}, i_{D3}, i_{D6}, i_{D7} and i_{D9} increase, and i_{D2}, i_{D4}, i_{D5}, i_{D8} and i_{D10} decrease in this mode. The output inductor voltages v_{Lo1}-v_{Lo5} are equal to $-V_o$ so that inductor currents i_{Lo1}-i_{Lo5} are decreasing. Since $i_{Lr1}(t_6)<0$, $i_{Lr2}(t_6)<0$,

$i_{Lr3}(t_6)>0$, $i_{Lr4}(t_6)<0$ and $i_{Lr5}(t_6)<0$, C_{r1} and C_{r3} are continuously discharged. C_{r1} and C_{r3} can be discharged to zero voltage if the energy stored in L_{r1}-L_{r5} is greater than the energy stored in C_{r1}-C_{r4}.



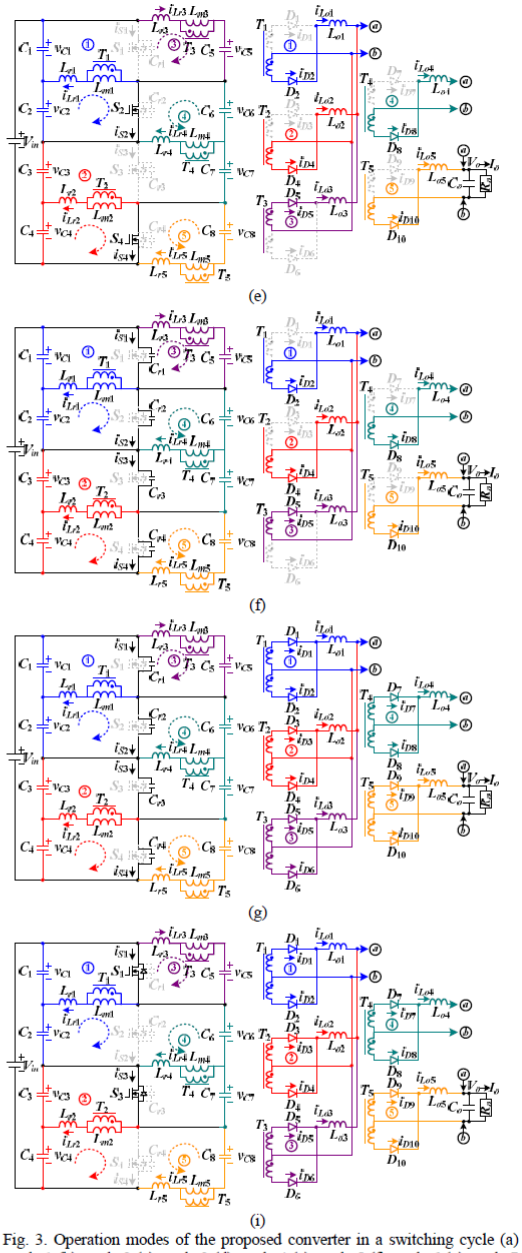


Fig. 3. Operation modes of the proposed converter in a switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8.

***Mode 8* [t_7 - t_0+T_s]:** Mode 8 starts at time t_7 when v_{Cr1}=v_{Cr3}=0, v_{Cr2}=v_{C1}+v_{C2} and v_{Cr4}=v_{C3}+v_{C4}. Since $i_{Lr1}(t_7)<0$, $i_{Lr2}(t_7)<0$, $i_{Lr3}(t_7)>0$, $i_{Lr4}(t_7)<0$ and $i_{Lr5}(t_7)<0$, the anti-parallel diodes of

S_1 and S_3 are conducting. S_1 and S_3 can be turned on at this moment to achieve ZVS. Since diodes D_1-D_{10} are still conducting, the inductor voltages can be obtained as $v_{Lr1}=v_{C1}$, $v_{Lr2}=v_{C3}$, $v_{Lr3}=-v_{C5}$, $v_{Lr4}=v_{C7}$, $v_{Lr5}=v_{C3}+v_{C4}-v_{C8}$ and $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=v_{Lo5}=-V_o$. Thus, i_{Lr1}, i_{Lr2}, i_{Lr4}, i_{Lr5} increase and i_{Lr3} and i_{Lo1}-i_{Lo5} decrease in this mode. At time t_0+T_s, i_{D2}, i_{D4}, i_{D5}, i_{D8} and i_{D10} are decreased to zero ampere. Then the circuit operations of the proposed converter in a switching cycle are completed.

IV. Converter Performance Analysis

There are eight operating modes in the proposed converter for every switching cycle. The transfer power from input voltage to output load through five PWM circuits is related to duty cycle of power MOSFETs. Each circuit provides one-fifth of rated output power. The duty cycle of S_1 and S_3 is δ and the duty cycle of S_2 and S_4 is 1-δ. In generally, the charge/discharge times of C_{r1}-C_{r4} in modes 2, 3, 6 and 7 are less than the time interval in the other modes. To simplify the system analysis in steady state, only modes 1, 4, 5 and 8 are considered in the following. Based on the volt-second balance on (L_{r1} and L_{m1}), (L_{r2} and L_{m2}), (L_{r3} and L_{m3}), (L_{r4} and L_{m4}) and (L_{r5} and L_{m5}) in steady state, the average capacitor voltages V_{C1}-V_{C8} can be derived as:

$$V_{C1}=V_{C3}=V_{C5}=V_{C7}=(1-\delta)V_{in}/2 \quad (1)$$

$$V_{C2}=V_{C4}=V_{C6}=V_{C8}=\delta V_{in}/2 \quad (2)$$

It can be obtained that $V_{C1}+V_{C2}=V_{C3}+V_{C4}=V_{C6}+V_{C7}=V_{in}/2$. In mode 4, the inductor current variations Δi_{Lr1}-Δi_{Lr5} are equal to $2I_o/(5n)$. The time interval in mode 4 is given in (9).

$$\Delta t_{34}=t_4-t_3\approx\frac{2I_oL_r}{5nv_{C2}}=\frac{2I_oL_r}{5nv_{C4}}=\frac{2I_oL_r}{5n(v_{C1}+v_{C2}-v_{C5})}$$
$$=\frac{2I_oL_r}{5nv_{C6}}=\frac{2I_oL_r}{5nv_{C8}}=\frac{4I_oL_r}{5n\delta V_{in}} \quad (3)$$

In mode 4, S_2, S_4 and D_1-D_{10} are conducting so that no power is delivered from input voltage to output load. The duty loss in mode 4 is obtained in (10).

$$\delta_{loss,4}=\frac{\Delta t_{34}}{T_s}=\frac{4I_oL_rf_s}{5n\delta V_{in}} \quad (4)$$

Similarly, the duty loss in mode 8 can be expressed as

$$\delta_{loss,8}=\frac{\Delta t_{70}}{T_s}=\frac{2I_oL_rf_s}{5nv_{C1}}=\frac{4I_oL_rf_s}{5n(1-\delta)V_{in}} \quad (5)$$

In operation mode 1, $v_{Lo1}\approx v_{C1}/n-V_o$, $v_{Lo2}\approx v_{C3}/n-V_o$, $v_{Lo3}\approx v_{C5}/n-V_o$, $v_{Lo4}\approx v_{C7}/n-V_o$ and $v_{Lo5}=(v_{C3}+v_{C4}-v_{C8})/n-V_o$. In operation mode 4, $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=v_{Lo5}=-V_o$. In operation mode 5, $v_{Lo1}\approx v_{C2}/n-V_o$, $v_{Lo2}\approx v_{C4}/n-V_o$, $v_{Lo3}\approx(v_{C1}+v_{C2}-v_{C5})/n-V_o$, $v_{Lo4}\approx v_{C6}/n-V_o$ and $v_{Lo5}=v_{C8}/n-V_o$. In operation mode 8, $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=v_{Lo5}=-V_o$. Based on the volt-second balance on L_{o1}-L_{o5}, the DC voltage gain of the proposed converter in steady state is obtained as

$$V_o=\frac{V_{in}}{n}\delta(1-\delta)-\frac{4L_rI_of_s}{5n^2}-V_f \quad (6)$$

where V_f is the voltage drop on diode of D_1-D_{10}. Applying the current-second balance on capacitances C_1-C_8, the average magnetizing currents of L_{m1}-L_{m5} can be obtained.

$$I_{Lm1}=I_{Lm2}=I_{Lm4}=I_{Lm5}=\frac{(1-2\delta)I_o}{5n} \quad (7)$$

$$I_{Lm3}=\frac{(2\delta-1)I_o}{5n} \quad (8)$$

The ripple currents on L_{m1}-L_{m5} are illustrated as:

$$\Delta i_{Lm}=\frac{V_{C1}(\delta-\delta_{loss,8})T_s}{L_m}=\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(5n)}{2L_m} \quad (9)$$

The ripple current on L_{o1}-L_{o5} are expressed as:

$$\Delta i_{Lo}=\frac{[\frac{(1-\delta)(1-2\delta)V_{in}}{2n}+\frac{4L_rI_of_s}{5n^2}](\delta-\frac{4L_rI_of_s}{5nV_{in}(1-\delta)})T_s}{L_o} \quad (10)$$

The average diode currents are expressed as:

$$I_{D1}=I_{D3}=I_{D6}=I_{D7}=I_{D9}\approx\delta I_o/5 \quad (11)$$

$$I_{D2}=I_{D4}=I_{D5}=I_{D8}=I_{D10}\approx(1-\delta)I_o/5 \quad (12)$$

The voltage stresses of D_1-D_6 are expressed as:

$$v_{D1,stress}=v_{D3,stress}=v_{D6,stress}=v_{D7,stress}=v_{D9,stress}$$
$$\approx\frac{2V_{C2}}{n}=\frac{\delta V_{in}}{n} \quad (13)$$

$$v_{D2,stress}=v_{D4,stress}=v_{D5,stress}=v_{D8,stress}=v_{D10,stress}$$
$$\approx\frac{2V_{C1}}{n}=\frac{(1-\delta)V_{in}}{n} \quad (14)$$

The root-mean-square (rms) currents of S_1-S_4 are approximately expressed as:

$$i_{S1,rms}=i_{S3,rms}\approx\frac{(1-\delta)I_o}{n}\sqrt{\delta} \quad (15)$$

$$i_{S2,rms}=i_{S4,rms}\approx\frac{\delta I_o}{n}\sqrt{1-\delta} \quad (16)$$

The voltage stresses of S_1-S_4 are equal to $V_{in}/2$. At t_1, i_{Lr1}-i_{Lr5} are approximately given as:

$$i_{Lr1}(t_1)=i_{Lr2}(t_1)=i_{Lr4}(t_1)=i_{Lr5}(t_1)$$
$$\approx i\frac{(1-2\delta)I_o}{5n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(5n)}{4L_m}$$
$$+\frac{I_o}{5n}+[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{5n^3}](\delta-\frac{4L_rI_of_s}{5nV_{in}(1-\delta)})\frac{T_s}{2L_o} \quad (17)$$

$$i_{Lr3}(t_1)\approx\frac{(2\delta-1)I_o}{5n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(5n)}{4L_m}$$
$$-\frac{I_o}{5n}-[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{5n^3}](\delta-\frac{4L_rI_of_s}{5nV_{in}(1-\delta)})\frac{T_s}{2L_o} \quad (18)$$

At t_5, i_{Lr1}-i_{Lr5} are approximately expressed as:

$$i_{Lr1}(t_5)=i_{Lr2}(t_5)=i_{Lr4}(t_5)=i_{Lr5}(t_5)$$
$$\approx\frac{(1-2\delta)I_o}{5n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(5n)}{4L_m}$$
$$-\frac{I_o}{5n}+[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{5n^3}](\delta-\frac{4L_rI_of_s}{5nV_{in}(1-\delta)})\frac{T_s}{2L_o} \quad (19)$$

$$i_{Lr3}(t_5)\approx\frac{(2\delta-1)I_o}{5n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(5n)}{4L_m}$$
$$+\frac{I_o}{5n}-[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{5n^3}](\delta-\frac{4L_rI_of_s}{5nV_{in}(1-\delta)})\frac{T_s}{2L_o} \quad (20)$$

Capacitors C_{r2} and C_{r4} can be discharged to zero voltage if the energy stored in L_{r1}-L_{r5} at time t_1 is greater than the

energy stored in C_{r1}-C_{r4} in modes 2 and 3. The ZVS condition of S_2 and S_4 can be given as

$$L_r \geq \frac{C_r V_{in}^2/2}{i_{Lr1}^2(t_1)+i_{Lr4}^2(t_1)/4+i_{Lr3}^2(t_1)} \quad (21)$$

Similarly, the ZVS condition of S_1 and S_3 can be obtained as

$$L_r \geq \frac{C_r V_{in}^2/2}{i_{Lr1}^2(t_5)+i_{Lr4}^2(t_5)/4+i_{Lr3}^2(t_5)} \quad (22)$$

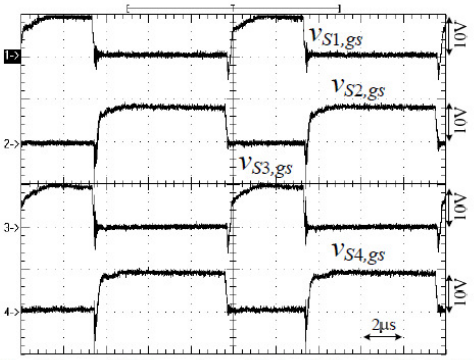


Fig. 4 Measured PWM waveforms of S_1-S_4 at full load and V_{in}=800V.

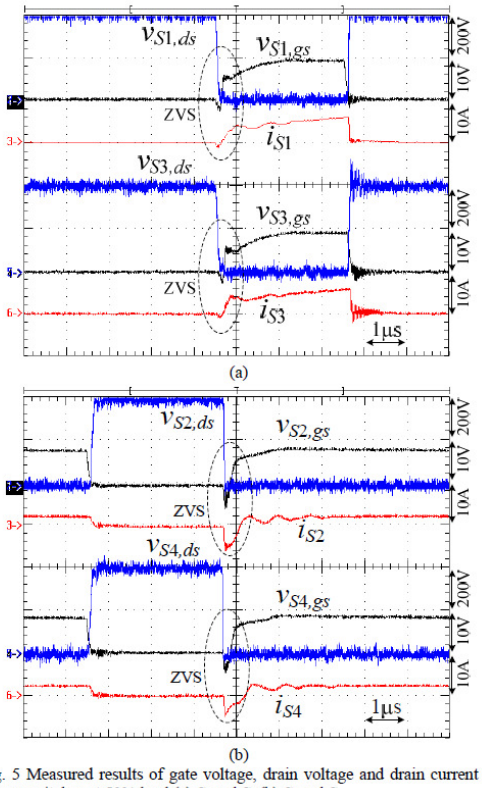


Fig. 5 Measured results of gate voltage, drain voltage and drain current of power switches at 50% load (a) S_1 and S_3 (b) S_2 and S_4.

V. Test Results

A laboratory prototype with 1.92kW rated power was constructed. The electric specifications of the prototype are V_{in}=750V-800V, V_o=24V, I_o=80 A and switching frequency f_s=100kHz. Fig. 4 shows the measured PWM waveforms of S_1-S_4 at full load. S_1 and S_3 have the same PWM waveforms, and S_2 and S_4 have the same PWM waveforms. The test results of gate voltage, drain voltage and drain current of S_1-S_4 at 50% load are illustrated in Fig. 5. The drain voltage is decreased to zero before power MOSFET is turned on. Therefore, power MOSFETs S_1-S_4 are all turned on under ZVS from 50% load. Fig. 6 gives the test results of primary inductor currents i_{Lr1}-i_{Lr5} at full load. It is clear that five inductor currents i_{Lr1}-i_{Lr5} are balanced each other. When S_1 and S_3 are turned on, i_{Lr1}, i_{Lr2}, i_{Lr4} and i_{Lr5} increase and i_{Lr3} decreases. On the other hand, i_{Lr1}, i_{Lr2}, i_{Lr4} and i_{Lr5} decrease and i_{Lr3} increases when S_1 and S_3 are turned off and S_2 and S_4 are turned on. Fig. 7 gives the measured capacitor voltages v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr6}+v_{Cr7} at full load. It is clear that these three voltages are balanced to V_{in}/2. The measured output inductor currents i_{Lo1} - i_{Lo5} and the total output inductor current i_{Lo1}+i_{Lo2}+i_{Lo3}+i_{Lo4}+i_{Lo5} at full load are given in Fig. 8. These five output inductor currents i_{Lo1} - i_{Lo5} are balanced.

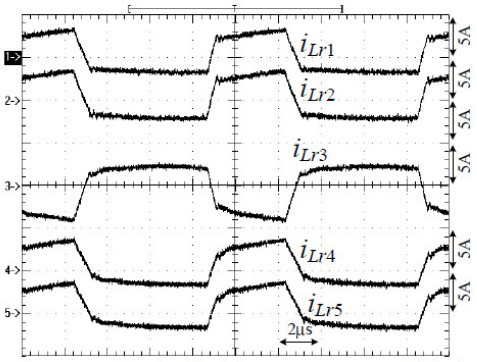


Fig. 6 Measured results of the inductor currents i_{Lr1}-i_{Lr5} at full load.

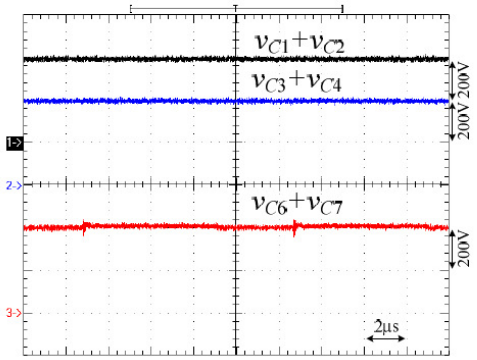


Fig. 7 Measured capacitor voltages v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr6}+v_{Cr7} at full loadV.

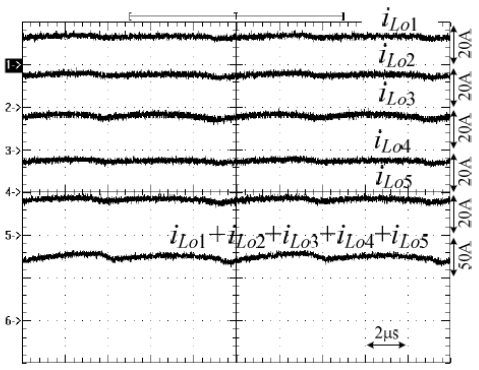


Fig. 8 Measured the secondary side currents at full load.

VI. Conclusion

A new DC/DC converter with five APWM circuits is presented for medium voltage and high load current applications. The series half-bridge circuits are adopted to limit the voltage stress of MOSFETs at $V_{in}/2$. Switching capacitor circuit is used to balance input spilt capacitor voltages. Five APWM circuits with the same power switches are adopted at the primary side to reduce the switch counts. Each circuit provides one-fifth of load power to secondary side so that the current stress of passive components and transformer windings are reduced. Compared to the conventional parallel three-level DC/DC converter, the proposed converter has less power MOSFETs counts. APWM scheme is adopted to generate switching signals of MOSFETs. Based on the resonant behavior by output capacitances of MOSFETs and resonant inductances at the transition interval, all MOSFETs can be turned on at ZVS form 50% load to full load. The system analysis, converter performance and design example of the proposed converter are discussed in detail. Finally, experimental verifications are provided to verify the effectiveness of the converter.

Acknowledgment

This project is supported by the National Science Council of Taiwan under Grant NSC 102-2221-E-224 -022 -MY3.

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