出席國際學術會議心得報告

報告名稱	出席 2014 ISEEE 國際會議並發表論文		
出國人員姓名	羅有龍	服務機構及職稱	國立高雄師範大學電子工程學系副教授
會議時間	103 年 04 月 26 日 至 103 年 04 月 28 日	會議地點	日本-北海道
會議名稱	2014 International Conference on Information Science, Electronics and Electronics Engineering		
發表論文題目	一個以延遲鎖定迴路為基礎的低相位雜訊全數位可程式化之時脈產生器 A Low Phase Noise All-Digital Programmable DLL-Based Clock Generator		

報告內容:

本人出席 2014 ISEEE 國際會議，此會議主要是由 IEEE Sapporo Section, Japan 贊助協辦，於日本北海道札幌舉辦。本次會議的領域主要包含有 Computer and Information Science 及 Electronics and Electrical Engineering 兩大領域，日期為 103 年 04 月 26 日至 103 年 04 月 28 日共計三天，開會的地點在札幌市的王子飯店。

此次會議安排三場精彩的 Keynote Speech，第一個講者是 Ivan Stojmenovic，他是 IEEE Fellow 來自 University of Ottawa, Canada，講演的題目為 Big Data in Social Networks；第二個講者是 Nirwan Ansari，他也是 IEEE Fellow 來自 New Jersey Institute of Technology, USA，講演的題目為 Greening At The Edges (GATE)；第三個講者是 Pin-Han Ho，他是台灣人，來自 University of Waterloo, Canada，講演的題目為 Broadcast of Superimposed Multi-resolution Content with User and Channel。

此次會議參與的人員來自許多國家，其中以亞洲國家居多，而國內參與的學者也不少，有分別來自中山大學、高雄大學、海洋大學、嘉義大學、元智大學、台灣科技大學、雲林科技大學及高雄第一科技大學等等。

我們所發表的論文被安排至會議的第三天下午，為口頭報告議程，該場次的 Session Chair 剛好是來自台灣海洋大學的李教授，而我們發表的題目為 A Low Phase Noise All-Digital Programmable DLL-Based Clock Generator，報告過程相當順利。

在會議過程中也與其他學者討論相關的技術，除了可以看到相近領域的研究發表外，也接觸到不同領域的研究，因此，參與此次會議對本人有相當的獲益，更有助於個人未來研究的深度及應用面的提升。

論文的中文簡介

一個以延遲鎖定迴路為基礎的低相位雜訊全數位可程式化之時脈產生器

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***摘要*—本論文提出一個以延遲鎖定迴路為基礎的低相位雜訊全數位可程式化之時脈產生器，此晶片採用 0.18 微米、1.8V 電壓的標準製程實現。整體電路主要是由一個多相位的延遲鎖定迴路及一個可程式化控制的頻率倍頻器所組成。量測結果表示輸入頻率可以為 100 MHz 至 600 MHz，輸出頻率可以為 100 MHz 至 1.2GHz，當輸出頻率為 800 MHz 時，其相位雜訊在 1MHz 偏移頻率下為-112.36 dBc，其全部功率消耗為 23.87 mW，而晶片的面積為 0.14 mm^2。此提出的全數位式時脈產生器易於跟不同的製程整合並具有低相位雜訊及低功耗的特點。**

關鍵詞—延遲鎖定迴路，數位控制延遲線，多相位輸出，頻率倍頻器，時脈產生器。

原理及架構簡介

(1) 架構說明

以全數位延遲鎖定迴路為基礎之時脈倍頻器架構，如圖 1 所示，主要分為兩個區塊，一為全數位延遲鎖定迴路核心 (All-Digital Delay-Locked Loop Core, ADDLL)，另一個為頻率倍頻器 (Frequency Multiplier)。延遲鎖定迴路核心由初始電路 (Initial Circuit, IC)、粗/細調迴路 (Coarse / Fine Tune Loop)、數位控制延遲線 (Digital-Controlled Delay Line, DCDL) 組成。其中，粗調迴路包含相位比較器(Phase Comparator)、連續漸近式暫存器 (Successive Approximation Register, SAR)；細調迴路包含相位偵測器 (Phase Detector)、上下數計數器 (Up/Dn Counter)；頻率倍頻器主要電路包含倍頻選擇器 (Multiplier Selector)、脈波產生器 (Pulse Generator)、邊緣合成器 (Edge Combiner)。

(2) 原理說明

以全數位延遲鎖定迴路為基礎之時脈倍頻器操作原理是將輸入參考訊號 (Ref_clk) 輸入到初始電路、相位比較器、相位偵測器以及數位控制延遲線後，初始電路將產生 Start 訊號， 將 SAR 和 Up/Dn Counter 的初始值設定在中間值，以避免錯誤鎖定的發生；數位控制延遲線將產生 16 個均勻分布的相位輸出。並利用外部輸入訊號 B[2:0]來選擇回授訊號(Int_clk)是 DCDL 的第 N 輸出相位及倍頻器的頻率倍數。

回授訊號決定後，先由 PC 判別回授訊號和輸入參考訊號的領先落後關係，並產生比較訊號 (Comp)，使 SAR 做連續計數的動作並控制 DCDL 增加或減少延遲時間，直到訊號差落於 PC 的 鎖定範圍(Lock Window, tc)，PC 進入無法判別的區域，此時，粗調迴路為鎖定狀態，其鎖定訊號 (Ld) 為 High，並轉換成細調迴路開始追鎖。進入細調迴路後，改由 PD 判別回授訊號是領先或落後參考訊號，產生上數 (Up) 或下數 (Dn)訊號，使計數器做計數動作，直到兩訊號差落於 PD 的死區(Dead Zone, tf)，則計數器停止計數，且數位延遲鎖定迴路達到鎖定狀態。

延遲鎖定迴路核心電路鎖住後，DCDL 將提供時脈產生器 N 個輸出相位，以產生倍頻所需的脈波(BX& BXb)，再由邊緣合成器(Frequency Multiplier)將這些脈波進行合成，產生 0.5N 倍的輸出倍頻訊號(Clkout & Clkoutb)，在此架構中可以產生 1 到 8 倍等八種倍頻輸出。

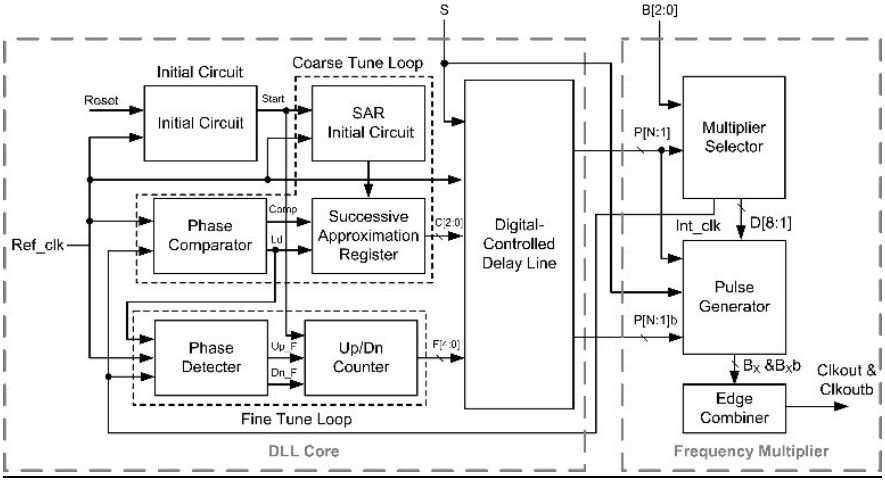

圖 1. 以全數位延遲鎖定迴路為基礎之時脈倍頻器

發表的論文

A Low Phase Noise All-Digital Programmable DLL-Based Clock Generator

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Abstract—**This paper proposes a low phase noise all-digital programmable DLL-based clock generator. The proposed clock generator is fabricated in a 0.18 µm standard CMOS process with a 1.8 V supply voltage. The proposed digital programmable DLL-based clock generator is easy migration over different processes and low power dissipation. The measurement results show that the input and output frequency ranges can operate 100 MHz ~ 600 MHz and 100 MHz ~ 1.2 GHz, respectively. At 800 MHz, the phase noise is -112.36 dBc @ 1MHz offset frequency. The total power consumption of the clock generator is 23.87 mW, and the active die area of the clock generator is 0.14 mm^2.**

Keywords*—*Delay-Lock Loop (DLL); digital control delay line; multiphase; frequency multiplier; clock generator

I. INTRODUCTION

In recent years, there have been increasing demands on clock generators capable of providing multiple-frequency clock signals in a wide frequency band for high-speed microprocessors, clock/data recovery (CDR) and mobile communication systems. Delay-locked loop (DLL)-based clock generators present strong advantages over conventional phase locked loop (PLL)-based approaches: better phase noise performance, robustness under robustness under process, voltage and temperature (PVT) variations, are easier to design, and fast settling times, and occupy smaller area due to a simpler loop filter.

However, in conventional analog DLL-based clock generators, the power consumption of the frequency multiplier is large as compared to the other blocks. Besides, conventional analog DLL-based clock generator uses capacitors to form low-pass filter which would occupy large chip area. Conversely, the digital DLL-based clock generator is easy migration over different processes and low power dissipation. Therefore, the all-digital DLL-based clock generator will become more important in the future [1]-[4].

In this paper, an all-digital low phase noise programmable DLL-based clock generator is proposed. To resolve the power consumption and large chip area in conventional analog DLL-based clock generator, it consists of digital control delay line, pulse generator, multiplier selector, and edge combiner. Moreover, clock generator can programmable by external bits to produce ×1 ~ ×8 of the reference frequency, operating over the widest frequency range among the various programmable frequency multipliers. Since the proposed clock generator occupies a small area and low power dissipation, it is quite attractive for system-on-a-chip (SoC) applications with dynamic frequency scaling.

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This paper is arranged as follows. Section II briefly overview the architecture of proposed all-digital low phase noise programmable DLL-based clock generator. Circuit description is presented in Section III. In Section IV, experimental result, chip micrograph, and performance comparison are presented. Finally, Conclusions are presented in Section V.

II. OVERALL ARCHITECTURE

The architecture of the proposed all-digital programmable DLL-based clock generator is shown in Fig. 1. It consists of DLL core and frequency multiplier. The DLL core consists of an initial circuit, coarse tune loop, fine tune loop, and digital- controlled delay line (DCDL). The course tune is composed of phase comparator (PC) and successive approximation register (SAR) [6]-[8]. And fine tune is composed of phase detector (PD) [9] and up/down counter [12] [13]. Frequency multiplier comprises multiplier selector, pulse generator and edge combiner.

The reference signals (Ref_clk) inject the reference clock to initial circuit, phase detector and digital control delay line to make a start signal that initial SAR and up/down counter at the mid to avoid harmonic locking, stuck locking. At the same time, sixteen uniform phases will be produced by digital control delay line. It can choose different feedback signals (Int_clk) to produce several multiplier by controlling the external input signal.

After the Int_clk has been chosen, feedback signal is compared with the Ref_clk by PC. If the Ref_clk is in the lead, the Comp signal will be high. In contrast, if the Ref_clk fall behind with the Int_clk, the Comp signal will be low. The Comp signal make SAR to control the delay time of the

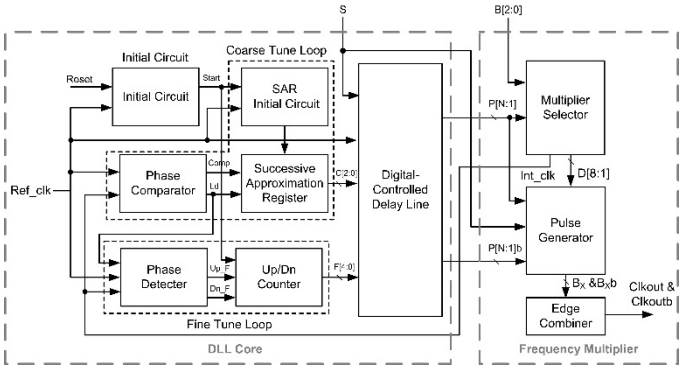

Fig. 1. The architecture of the proposed all-digital programmable DLL-based clock generator.

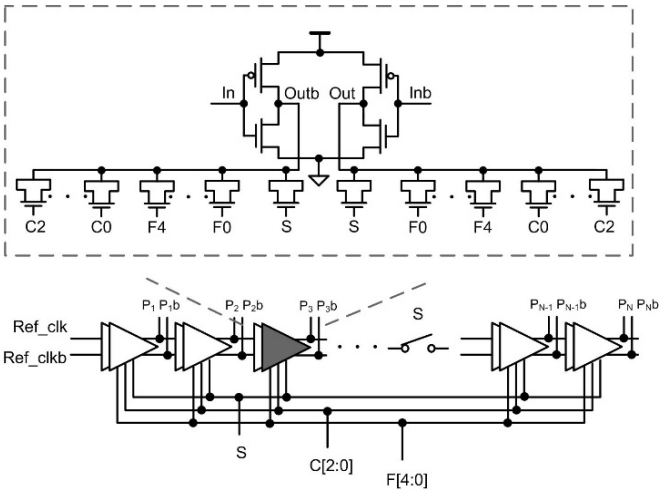

Fig. 2. The architecture of digital-controlled delay line.

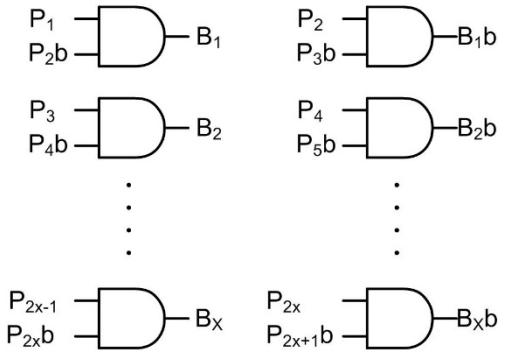

Fig. 3. The architecture of pulse generator.

delay loop until the PC can't distinguish whether the Int_clk lead or lag. At the moment course tune is locking that lock signal (LD) is high. After the PC is locking, the fine tune phase detector (PD) starts working. The fine tune PD distinguish whether the Int_clk lead or lag to the Ref_clk and generating up/dn signals to control up/down counter to adjust the delay time of delay loop. When the phase difference of the Ref_clk and Int_clk is within the dead zone of the PD, then the PD will stop counting.

III. Circuit Description

A. Digital-Controlled Delay Line (DCDL)

The adopted delay cell is shown in Fig. 2. DCDL consists of differential delay cells. Every delay cell is made up of two identically delay elements. It produces different delay to make sixteen phase output.

The digital-controlled delay line comprise 8-bit delay element. Three-bit C[2:0] is from the course loop that control by binary weight to achieve wide delay range. And the five-bit F[0:4] is from fine loop that control by thermal code. It provides high resolution delay time to reduce static phase error.

B. Pulse Generator

The architecture of pulse generator is shown in Fig. 3. It's made up of AND gate which generated various clocks. The clocks P1 and P2b use AND operation in pulse generator to made B1 pulse. Likewise, the clocks P2 and P3b use AND operation in pulse generator to made B1b pulse and so on. The following is function of pulse generator:

$$Bx = P_{2X-1} \cdot P_{2X}b$$

$$Bxb = P_{2X} \cdot P_{2X+1}b \quad \text{where } x = 1 \sim 8$$

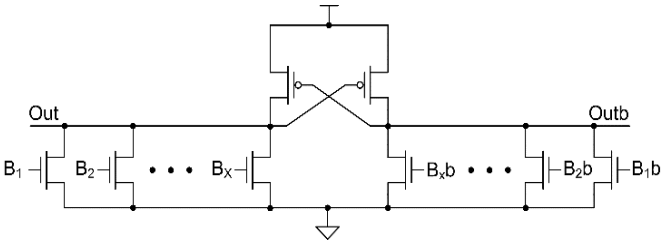

Fig.4. The architecture of edge combiner.

Table I: The truth table of pulse generator

B2	B1	B0	Int_clk	Multiplier
0	0	0	P2	X1
0	0	1	P4	X2
0	1	0	P6	X3
0	1	1	P8	X4
1	0	0	P10	X5
1	0	1	P12	X6
1	1	0	P14	X7
1	1	1	P16	X8

Table II: The truth table of edge combiner

B_x	B_xb	Out	Outb
1	0	0	1
0	1	1	0

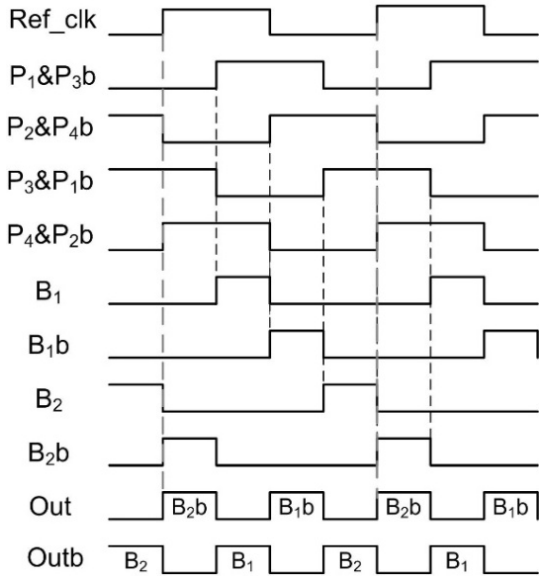

Fig. 5. The timing diagram of 2× reference frequency.

C. Multiplier Selector and Edge Combiner

The multiplier selector use three external bits to control pulse generator what it contribute different clocks. The truth

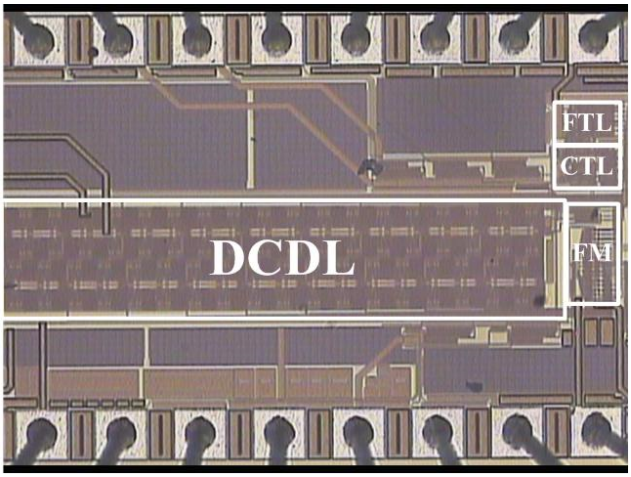

Fig. 6. The chip micrograph of the proposed clock generator.

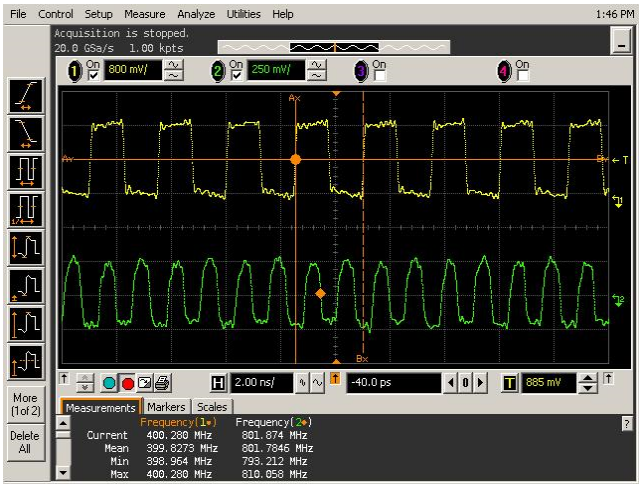

Fig. 7. 800 MHz for 2× reference frequency.

table is shown in table I. The architecture of edge combiner is shown in Fig. 4. When the Bx is high then the Bxb will be low. On the other hand, when the Bx is low then the Bxb will be low. The truth table of edge combiner is shown in Table II. After the edge combiner completes the synthesis procedure, the out signals Out and Outb will be produce. Following is the function of edge combiner:

$$Out = \overline{B1 + B2 + \cdots Bx}$$

$$Outb = \overline{B1b + B2b + \cdots Bxb} \quad \text{where } x = 1 \sim 8$$

The timing diagram of 2× reference frequency is shown in Fig. 5. When the B[2:0] is "001", the P1 and P3b, P2 and P4b, P3 and P1b, P4 and P2b also have same output clock. Finally, the B1, B1b, B2, B2b will be operated by edge combiner to output clock 2× what the reference clock is input.

IV. Experiment Result

The proposed low phase noise all-digital programmable DLL-based clock generator was fabricated in a 0.18-μm CMOS process with a 1.8 V supply voltage. Fig. 6 shows the chip micrograph of the proposed clock generator. The active die area of the chip is 0.14 mm^2. The frequency multiplier generates 2×, 3× 5×, 8× of reference clock, as shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10, respectively. The spectrum of the clock generator is shown in Fig. 11. The phase noise is -112.36 dBc@1 MHz offset frequency, as shown in Fig. 12. The comparison between the proposed clock generator and previous work is displayed in Table III. The proposed clock generator can provide an odd multiplication factor of up to 8. Moreover, the proposed clock generator has better performance in phase noise.

Fig. 8. 1.2 GHz for 3× reference frequency.

Fig. 9. 1 GHz for 5× reference frequency.

Fig. 10. 1.2 GHz for 8× reference frequency.

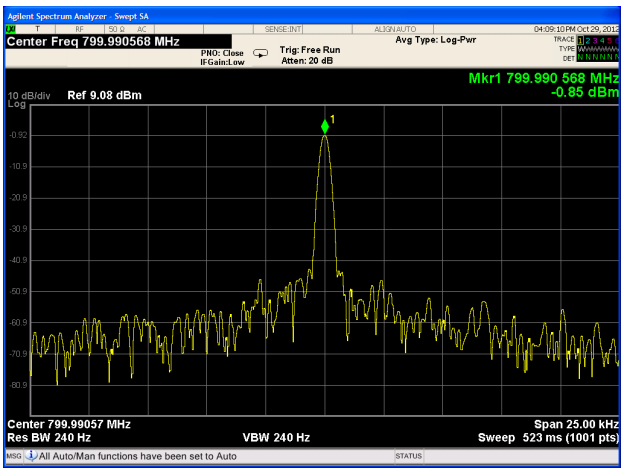

Fig. 11. Measured output spectrum of the proposed clock generator.

Fig. 12. Measured phase noise plot.

V. Conclusion

The low phase noise all-digital programmable DLL-based clock generator is proposed that can be applied to microchip, clock data recovery, mobility communication system and SoC. The proposed clock generator can produce ×1~×8 clock what it provides several clocks to different system. The chip is fabricated in a 0.18 µm standard CMOS process with a 1.8 V supply voltage. The active die area of the chip is 0.14mm^2. The proposed clock generator can operate with input clock range is 100 MHz ~ 600 MHz and the output range is 100 MHz ~ 1.2 GHz. The phase noise is -112.36 dBc @ 1MHz offset frequency.

Acknowledgment

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Table III: Performance comparison with prior works

	[1]	[2]	**This work**
Process	0.18-µm	0.25-µm	**0.18-µm**
Supply Voltage	1.8 V	2.5 V	**1.8 V**
Programmability	×4, ×8, ×12, ×24	No	**×1~×8**
Output Range	30 MHz ~ 2.16 GHz	120 MHz ~ 1.2 GHz	**100 MHz ~ 1.2 GHz**
Phase Noise	-82.6 dBc @ 1 KHz -87.7 dBc @ 10 KHz -99.8 dBc @ 100 KHz	-88 dBc @ 10 KHz	**-73.95 dBc @ 1KHz -89.83 dBc @ 10KHz -108.26 dBc @100 KHz -112.36 dBc @ 1MHz**
Power Consumption	16.2 mW @ 2.16 GHz	52.5 mW @ 1.2 GHz	**23.87 mW@ 800 MHz**
Active Area	0.051 mm^2	0.13 mm^2	**0.14 mm^2**

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