出國報告（出國類別：其他-國際會議）

參加「二〇一四年IEEE ICIEA國際研討會」出國報告

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派赴國家：中國/杭州
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摘要

出席二〇一四年 IEEE-ICIEA 國際會議,此行主要目的是向國際間電力電子專家學者介紹國內在電力電子方面之研究成果，與國外學者交換電源轉換技術之發展，與專家學者討論高效率電源轉換器術與再生能源應用與研究趨勢。聆聽各國學者與業界工程師在電力電子技術、能源控制、智慧控制、電動機研究趨勢與再生能源應用等最新研究報告。研討會期間與研究領域相關的國內外研究學者與專家相互討論能源轉換技術與再生能源新技術等相關問題，藉以提升在電力電子研究方面的深度與廣度。研討會中，針對筆者發表數種不同方法的諧振式直流對直流轉換器架構與高壓輸入之轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此種電路架構都具有零電壓切換技術及高效率電路等優點，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能。此次參加國際研討會獲得很多國外目前之研究成果，也詳細向國外學者介紹台灣之研究績效。

目次

一、 目的

參加二〇一四年IEEE-ICIEA國際研討會之主要目的為1.發表實驗室2013年之研究成果，2.學習世界各專家學者與研究單位的研究方向與成果，3.與國際學者廣泛討論再生能源之發展趨勢，4.向各國學者說明與介紹台灣目前在高效率電源轉換器與再生能源技術研究之成果。

二、 過程

二〇一四年IEEE-ICIEA國際研討會在中國/杭州召開，會議時間自6月8日至6月11日。主辦單位為IEEE工業電子協會，承辦單位為中國浙江科技大學。ICIEA國際學術研討會是每年舉辦一次關於電力電子、能源科技、控制系統與通訊工程方面之國際學術研討會，每年會議在世界各國家舉辦(明年會議將在五月於紐西蘭/奧克蘭市舉辦)。此次研討會投稿篇數為六百多篇，投稿全文經三位審稿者無記名審查，通過審查共有四百零五篇論文於會議中分三十個場次發表。會議中安排有六場主題演講，會議內容共有27個時段論文的口頭發表及3個時段海報張貼方式的論文發表。

6/9 日至 6/11 日參加各場次之論文發表會，筆者於研討會會中發表四篇論文:

1. Resonant Converter with Flying Capacitors – Analysis and Experiments
2. Asymmetric PWM Converter for High Load Current Application
3. Interleaved Resonant Converter with Flying Capacitor
4. Half-Bridge ZVS Converter with Three Resonant Tanks

筆者論文中發表四種不同方法的高效率高壓直流轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此四種電路架構都具有流電壓及零電流切換技術，此兩種電路採用不同之控制方法，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能，發表文章獲得與會各國教授熱烈討論與互相交流。

三、 心得

2014 年 IEEE-ICIEA 為世界上有關電力電子、能源科技、控制系統與通訊工程方面重要會議之一。本次會議共有四百零五篇篇論文，中國是投稿篇數較多的國家，台灣在此國際研討會的參與度相當積極，為提高台灣之學術地位及能見度，需國科會、教育部及各學術單位的補助以參加此等會議。在本次的會議中可以看出論文廣度加大，在會議中認識其他國家的人士，彼此交換心得，對於開拓視野、提升研究品質有莫大的幫助。此次會議之人員安排及會議過程順利，茲將出席本次會議心得分述如下：

1. 台灣學者在研究深度上與各國相比較，表現很好。
2. 高效率電源器術在會議中討論踴躍，消費型電源技術有多篇在會議中發表。
3. 會中與各國專家學者交換高效率電源轉換器與再生能源技術，獲益良多。
4. 與中國、日本及韓國學者在大會上廣泛互動與討論研究方向。

5. 此次會議中較多研究論文發表集中再生能源發電系統與消費型電源產品，利用高效能轉換器技術讓整體電源技術之效率提升。

6.雲端電源技術之發展，在此次研討會中也是被討論主題之一。

7.大型高瓦數電動機控制系統在研討會中也受到相當之重視。

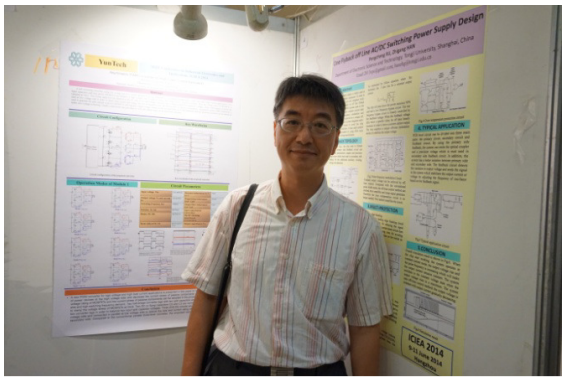
四、 建議事項

IEEE-ICIEA 國際會議為 IEEE 有關電力電子、能源科技、控制系統與通訊工程方面重要的國際會議，所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對工業升級及發展高科技所需的高效率電源及驅動系統之發展，均有相當的影響。由於參與類似的學術性會議非常重要，故有以下建議:

1. 鼓勵學者積極參與國際學術會議。
2. 政府應對此領域之研究多作投資。
3. 中國學者出席國際研討會近幾年相當積極，人數超出台灣學者很多，台灣在此方面要多鼓勵國內學者出席介紹台灣教學研究成果。

五、 附錄

與研究生於大會會場



論文發表現場

Resonant Converter with Flying Capacitors – Analysis and Experiments

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***Abstract*—This paper presents a new resonant converter to achieve soft switching on power devices. Two full-bridge converters are connected in series to clamp the voltage stress of power switches at $V_{in}/2$. Thus, power MOSFETs with 650V voltage rating can be used for 1300V input voltage applications. Two flying capacitors are connected on the AC side of two full-bridge converters to automatically balance two split input capacitor voltages in every switching cycle. Two resonant tanks are used in the proposed converter to share load current and reduce the current stress of passive and active components. If the switching frequency is less than the series resonant frequency of the resonant tanks, power MOSFETs can be turned on under zero voltage switching and rectifier diodes can be turned off under zero current switching. The switching losses on power MOSFETs are reduced and the reverse recovery loss is improved. Experiments with a 1.5kW prototype are provided to demonstrate the performance of the proposed converter.**

***Keywords*—Resonant converter, ZVS**

I. INTRODUCTION

Three-level converters or inverters have been proposed for high voltage applications such as high speed railway electrical system [1], three-phase high power factor correction converter, ship electric power distribution system [2], reactive power compensator [3]-[5] and AC motor systems [6]-[8]. Three-level converters/inverters [3]-[8] with neutral-point diode clamp, capacitor clamp or series H-bridge topologies have been proposed and developed to decrease the voltage stress of power devices and increase the switching frequency. Thus, the size of passive components can be decreased. For modern power converters, the compact size, high power density and high circuit efficiency are normally demanded. Thus, three-level converters [9]-[14] with zero voltage switching (ZVS) have been proposed to reduce the switching losses on power devices at the desired load range. Based on the resonant behavior by the leakage inductance and the resonant capacitance, the power switches can be turned on under ZVS during the transition interval. However, the ZVS range of power switches is depended on load power and input voltage conditions. Thus, it is very difficult to design a ZVS three-level converter with a wide range of load condition. Recently, resonant converters [14]-[16] have been drawn attention due to its essential advantages of high conversion efficiency and wide ZVS range of load condition. If the switching frequency is less than the series resonant frequency, the rectifier diodes at the secondary side are operated under zero current switching (ZCS) and power switches are operated under ZVS turn-on. Thus, the reverse recovery losses of diode rectifier are improved and switching losses of power switches are reduced. However, the voltage stress of power switches in conventional resonant converter is equal to input DC bus voltage. In conventional three-level resonant converter [17]-[18], the input split DC voltages cannot be balanced automatically in every switching cycle.

This paper presents a new resonant converter to have the functions of low voltage stress of power switches, low switching losses and the balanced input capacitor voltages in every switching cycle. Two full-bridge resonant converters are connected in series at high voltage side to limit the voltage stress of power switch at $V_{in}/2$. The secondary sides of two full-bridge converters are connected in parallel to share load current and reduce the size of active and passive components. In order to balance two input capacitor voltages, two flying capacitors are connected between the AC sides of two full-bridge converter legs. Thus, the input capacitor voltages can be automatically balanced in each switching cycle. The pulse frequency modulation is adopted to regulate the output voltage. The input impedance of the resonant converter is controlled as an inductive load at the switching frequency. Thus, power switches can be turned on under ZVS with a wide range of load condition. If the switching frequency is lower than the series resonant frequency, then rectifier diodes can be turned off under ZCS. The system analysis, circuit characteristics and design example of the prototype circuit are discussed in detail. Finally, experiments are provided to demonstrate the performance of the proposed converter.

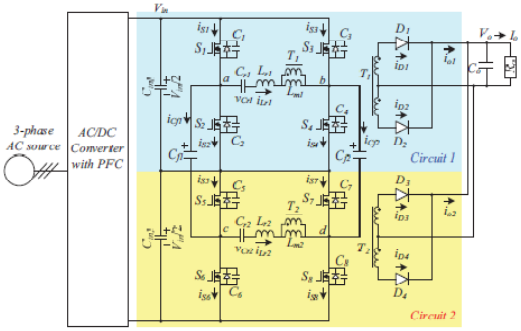

Fig. 1 Proposed ZVS converter with two full-bridge resonant circuits and two flying capacitors.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed converter is shown in Fig. 1. The front stage of this converter is a three-phase power factor corrector to achieve high power factor. The input DC bus voltage V_{in} of the second stage DC/DC

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converter is normally regulated at 750V-800V for a three-phase 480V AC voltage system. Two full-bridge resonant converters are connected in series at high voltage side to reduce the voltage stress of power switches and to achieve high circuit efficiency due to ZVS turn-on for each power switch. The secondary sides of these two converters are connected in parallel in order to reduce the current stress of passive and active components. In order to automatically balance two input split capacitor voltages v_{Cin1} and v_{Cin2}, two flying capacitors C_{f1} and C_{f2} are connected at the AC terminal points (a, c) and (b, d). Thus, two split capacitor voltages and two flying voltages are automatically balanced, $v_{Cin1}=v_{Cin2}=v_{Cf1}=v_{Cf2}=V_{in}/2$, in a switching cycle. C_{in1} and C_{in2} are input split capacitances. S_1-S_8 are power MOSFETs. L_{r1} and L_{r2} are resonant inductances. C_{r1} and C_{r2} are resonant capacitances. C_1-C_8 are output capacitances of S_1-S_8, respectively. D_1-D_4 are rectifier diodes at output side. L_{m1} and L_{m2} are the magnetizing inductances of transformers T_1 and T_2, respectively. C_{f1} and C_{f2} are flying capacitances. C_o is output capacitance. Two full-bridge resonant converters are used to regulate output voltage. The first resonant converter includes C_{in1}, S_1-S_4, C_1-C_4, C_{r1}, L_{r1}, T_1, D_1, D_2 and C_o. The components of the second resonant converter are C_{in2}, S_5-S_8, C_5-C_8, C_{r2}, L_{r2}, T_2, D_3, D_4 and C_o. C_{f1} and C_{f2} are used to balance v_{Cin1} and v_{Cin2} in every switching cycle. The voltage stress of each power switch is clamped at $V_{in}/2$. Therefore, MOSFETs with 500V or 600V voltage stress can be used at 800V input voltage condition. The pulse frequency modulation scheme is adopted to regulate output voltage. If the switching frequency is less than the series resonant frequency at full load and maximum input voltage case, power switches S_1-S_8 are turned on at ZVS and rectifier diodes D_1-D_4 are turned off at ZCS. Thus, the switching losses of power switches are reduced and the reverse recovery losses of rectifier diodes are improved.

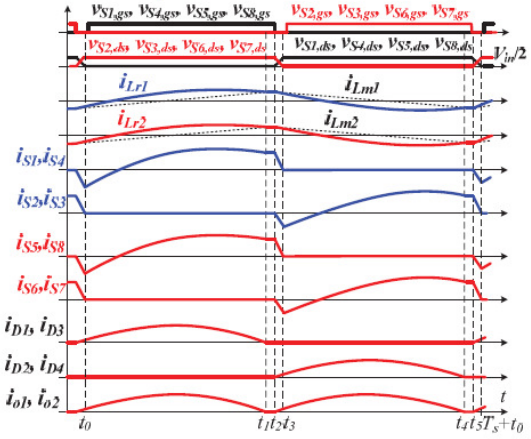


Fig. 2 Key waveforms of the proposed converter.

III. Operation Principle

In this section, the system analysis and operation principle of the proposed converter are discussed by the following assumptions. (1) Transformers T_1 and T_2 have the same magnetizing inductances $L_{m1}=L_{m2}=L_m$ and turns ratio $n=n_p/n_{s1}=n_p/n_{s2}$, (2) S_1-S_8 are ideal and have the same output capacitances $C_1=...=C_8=C_{oss}$, (3) diodes D_1-D_4 are ideal, (4) resonant inductances $L_{r1}=L_{r2}=L_r$, (5) resonant capacitances $C_{r1}=C_{r2}=C_r$, (6) C_o is large enough so that V_o is a constant voltage, (7) $V_{Cin1}=V_{Cin2}=V_{Cf1}=V_{Cf2}=V_{in}/2$, and (8) $C_{in1}=C_{in2}$ and $C_{f1}=C_{f2}$. Pulse frequency modulation is adopted to change the input impedance of the proposed converter such that the output voltage is regulated at the desired voltage value against the different input voltage and load conditions. Based on the on/off states of S_1-S_8 and D_1-D_4, six operating modes can be derived in a switching period. Fig. 2 shows the key PWM waveforms of the proposed converter. The duty cycle of S_1-S_8 is 0.5. S_1, S_4, S_5 and S_8 have the same PWM waveforms. In the same manner, S_2, S_3, S_6 and S_7 have the same PWM waveforms. However, the PWM waveforms of S_1 and S_2 are complementary each other. The equivalent circuits of each operation mode are shown in Fig. 3. Before time t_0, S_1-S_8, D_2 and D_4 are all in the off-state. Capacitors C_1, C_4, C_5 and C_8 are discharged, and C_2, C_3, C_6 and C_7 are charged.

Mode 1 **[$t_0 \le t < t_1$]:** At t_0, C_1, C_4, C_5 and C_8 are discharged to zero voltage. Since i_{Lr1} and i_{Lr2} are both negative, the anti-parallel diodes of S_1, S_4, S_5 and S_8 are conducting. Therefore, S_1, S_4, S_5 and S_8 can be turned on at this moment to achieve ZVS. The flying capacitor voltages $v_{Cf1}=V_{Cin1}$ and $v_{Cf2}=v_{Cin2}$. The voltage stresses of S_2 and S_3 are equal to V_{Cin1} and the voltage stresses of S_6 and S_7 are equal to V_{Cin2}. In resonant circuit 1, $i_{Lr1}>i_{Lm1}$ and diode D_1 conducts. Thus, $v_{Lm1}=nV_o$ and i_{Lm1} is increasing in this mode. C_{r1} and L_{r1} are resonant with the initial voltage $V_{in}/2-nV_o-v_{Cr1}(t_0)$. Similarly, C_{r2} and L_{r2} are resonant with the initial voltage $V_{in}/2-nV_o-v_{Cr2}(t_0)$ in the second resonant circuit and i_{Lm2} is also increasing. The input power is transferred to output load through (S_1, L_{r1}, T_1, S_4, D_1) in resonant circuit 1 and (S_5, L_{r2}, T_2, S_8, D_3) in resonant circuit 2.

Mode 2 **[$t_1 \le t < t_2$]:** At t_1, $i_{Lr1}=i_{Lm1}$ and $i_{Lr2}=i_{Lm2}$. Then diodes D_1-D_4 are all off in this mode. Since S_1 and S_4 are still conducting, C_{r1}, L_{r1} and L_{m1} are resonant in resonant circuit 1. In the same manner, S_5 and S_8 are still conducting such that C_{r2}, L_{r2} and L_{m2} are resonant in resonant circuit 2.

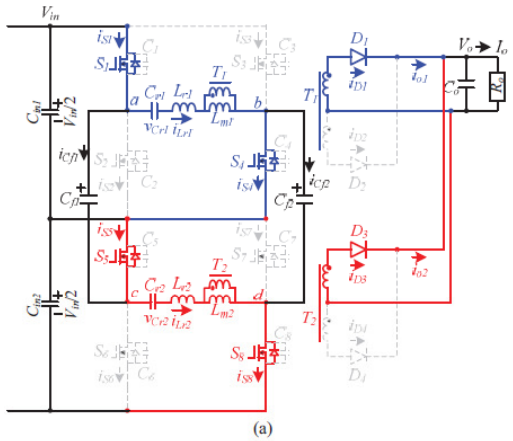
Mode 3 **[$t_2 \le t < t_3$]:** At t_2, S_1, S_4, S_5 and S_8 are turned off and diodes D_2 and D_4 are conducting. Thus $v_{Lm1}=v_{Lm2}=-nV_o$. The magnetizing currents i_{Lm1} and i_{Lm2} decrease with the slope of $-nV_o/L_m$. Since $i_{Lr1}(t_2)>0$ and $i_{Lr2}(t_2)>0$, C_1, C_4, C_5 and C_8 are charged and C_2, C_3, C_6 and C_7 are discharged. If the energy stored in L_{r1} and L_{r2} at t_2 is greater than the energy stored in C_1-C_8, then C_2, C_3, C_6 and C_7 can be discharged to zero voltage at time t_3.

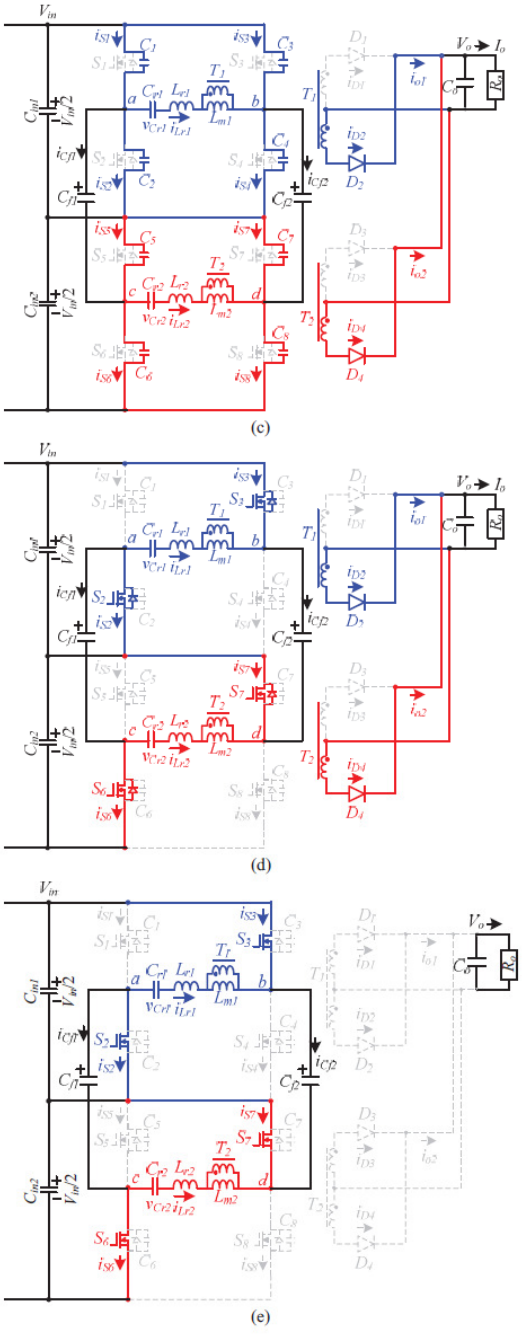
Mode 4 **[$t_3 \le t < t_4$]:** At t_3, C_2, C_3, C_6 and C_7 are discharged to zero voltage and the anti-parallel diodes of S_2, S_3, S_6 and S_7 are conducting. Before i_{Lr1} and i_{Lr2} are negative, S_2, S_3, S_6 and S_7 can be turned on at this moment under ZVS. Since D_2 and D_4 are conducting, $v_{Lm1}=v_{Lm2}=-nV_o$. Thus, i_{Lm1} and i_{Lm2} decrease in this mode. The voltage stresses of S_1 and S_4 are equal to V_{Cin1}, and the voltage stresses of S_5 and S_8 are equal to V_{Cin2}. The flying capacitor voltages $v_{Cf1}=V_{Cin2}$ and $v_{Cf2}=v_{Cin1}$. In circuit module 1, C_{r1} and L_{r1} are resonant with

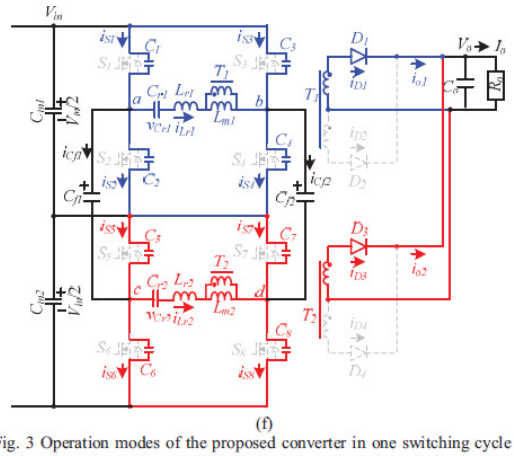
the initial voltage nV_o-V_{in}/2-$v_{Cr1}(t_3)$. Similarly, C_{r2} and L_{r2} are resonant with the initial voltage nV_o-V_{in}/2-$v_{Cr2}(t_3)$ in the second resonant circuit. The input power is transferred to output load through (S_3, L_{r1}, T_1, S_2, D_2) in resonant circuit 1 and (S_7, L_{r2}, T_2, S_6, D_4) in resonant circuit 2.

Mode 5 **[$t_4 \le t < t_5$]:** At t_4, $i_{Lr1}=i_{Lm1}$ and $i_{Lr2}=i_{Lm2}$. Thus, diodes D_1-D_4 are all off. Since S_2, S_3, S_6 and S_7 are still in the on-state, C_{r1}, L_{r1} and L_{m1} are resonant in circuit 1 and C_{r2}, L_{r2} and L_{m2} are resonant in circuit 2.The flying capacitor voltages $v_{Cf1}=V_{Cin2}$ and $v_{Cf2}=v_{Cin1}$ in this mode.

Mode 6 **[$t_5 \le t < T_s+t_0$]:** At t_5, S_2, S_3, S_6 and S_7 are turned off and diodes D_1 and D_3 are conducting. Magnetizing voltages $v_{Lm1}=v_{Lm2}=nV_o$. Thus, i_{Lm1} and i_{Lm2} increase in this mode. Since i_{Lr1} and i_{Lr2} are negative, C_1, C_4, C_5 and C_8 are discharged and C_2, C_3, C_6 and C_7 are charged. If the energy stored in L_{r1} and L_{r2} at t_5 is greater than the energy stored in C_1-C_8, then C_1, C_4, C_5 and C_8 can be discharged to zero voltage at time T_s+t_0. Then, the operating modes of the proposed converter in a switching cycle are completed.







(f)

Fig. 3 Operation modes of the proposed converter in one switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6.

IV. Circuit Characteristics and Design Example

The output voltage of the proposed converter is based on the pulse frequency modulation. Thus, the fundamental harmonic approach with variable switching frequency is used to approximately analysis the steady state of the proposed converter. The power transfer from input terminal to output load through two full-bridge resonant tanks is depended on the switching frequency. All harmonics of the switching frequency are neglected in the flowing discussion. Fig. 4 shows the equivalent circuit of the proposed converter for the derivation of steady state model. The equivalent circuit components in two resonant tanks are identical. Each resonant tank is supplied one-half of input power to output load. Since the duty ratio of each power switch is equal to 0.5, the input AC voltages v_{ab} and v_{cd} of resonant tanks are the square waveforms with two voltage levels $V_{in}/2$ and $-V_{in}/2$. The AC voltages v_{ab} and v_{cd} can be expressed as the fundamental frequency term and harmonics term.

$$v_{ac}(t)=v_{cd}(t)=\frac{2V_{in}}{\pi}\sin\omega_s t+\sum_{n=2}^{\infty}\frac{2V_{in}}{n\pi}\sin n\omega_s t=v_f+v_h \quad (1)$$

From (1), the fundamental root-mean-square (*rms*) value of v_{ab} and v_{cd} is equal to $\sqrt{2}V_{in}/\pi$. Due to the on-off states of D_1-D_4, the fundamental *rms* value of the magnetizing voltages is expressed as $v_{Lm1,rms}=v_{Lm2,rms}=2\sqrt{2}nV_o/\pi$. Since the average output current of each center-tapped rectifier is equal to $I_o/2$, the *rms* value of the secondary winding currents is equal to $i_{T1,s,rms}=i_{T2,s,rms}=\pi I_o/4\sqrt{2}$. Therefore, the load resistance R_o reflected to the transformer primary side can be expressed as:

$$R_{ac,1}=R_{ac,2}=R_{ac}=\frac{v_{Lm1,rms}}{i_{T1,rms,s}/n}=\frac{16n^2}{\pi^2}R_o \quad (2)$$

The resonant tank is excited by an effectively fundamental sinusoidal input voltage v_f and drives the effective AC resistive load R_{ac}. Pulse frequency modulation (PFM) scheme is adopted to regulate the AC voltage gain of the proposed converter. The AC voltage gain of the resonant tank can be expressed as:

$$|G_{ac}(f_s)|=1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2+Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2} \quad (3)$$

where $f_r=1/(2\pi\sqrt{L_rC_r})$, $Q=\sqrt{L_r/C_r}/R_{ac}$, $k=L_r/L_m$, $C_{r1}=C_{r2}=C_r$, $L_{r1}=L_{r2}=L_r$ and f_s is the switching frequency. The DC voltage gain G_{dc} of the proposed converter is given as:

$$G_{dc}=\frac{2n(V_o+V_f)}{V_{in}} \quad (4)$$

where V_f is the voltage drop on rectifier diodes D_1-D_4. If the input and output DC voltages are given, the operating switching frequency can be obtained by $G_{dc}=G_{ac}$.

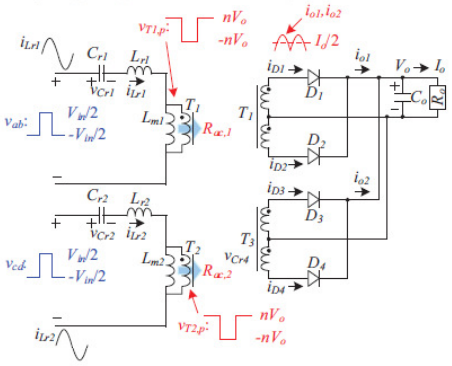


Fig. 4 Equivalent circuit of the proposed converter for the derivation of steady state model.

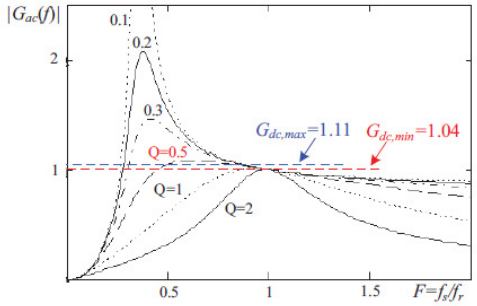


Fig. 5 Gain curves of proposed resonant converter with $V_{in,min}$=750V and $V_{in,max}$=800V.

A laboratory prototype is implemented with the following electric specifications: V_{in}=750*V*-800*V*, V_o=48*V*, P_o=1500*W*, series resonant frequency f_r=120*k*Hz. The primary and secondary winding turns of transformers T_1 and T_2 are 34 turns and 4 turns, respectively. Thus, the minimum and maximum DC voltage gains of resonant converter are expressed as:

$$G_{dc,\min}=\frac{2n(V_o+V_f)}{V_{in,\max}}=\frac{2\times(34/4)\times(48+1.1)}{800}\approx 1.04 \quad (5)$$

$$G_{dc,\max}=\frac{2n(V_o+V_f)}{V_{in,\min}}=\frac{2\times(34/4)\times(48+1.1)}{750}=1.11 \quad (6)$$

The AC equivalent resistance R_{ac} at full load condition are given as:

$$R_{ac}=\frac{16n^2R_o}{\pi^2}\approx 180\Omega \quad (7)$$

In the prototype circuit, the selected inductance ratio of L_r and L_m is $k=L_r/L_m=0.2$.The AC voltage gain curves of the proposed converter with different quality factor Q and frequency ratio F at $k=0.2$ are illustrated in Fig. 5. From Fig. 5, it is observed that the output voltage can be regulated if the quality factor Q≤0.5 at full load. Therefore, $Q=0.5$ at full load is selected in the prototype circuit. The AC voltage gain of the proposed converter at no load condition ($Q=0$) is given as:

$$|G_{ac}(f_s)|_{Q=0,f_s=\infty}\approx 1/(1+k)=1/(1+1/5)=0.83<G_{dc,\min} \quad (8)$$

Therefore, the output voltage V_o can be regulated at no load condition. Based on the derived R_{ac}, k, Q and f_r, the resonant inductances, the magnetizing inductances and the resonant capacitances can be obtained.

$$L_r=L_{r1}=L_{r2}=\frac{QR_{ac}}{2\pi f_r}=\frac{0.5\times 180}{2\pi\times 120\times 10^3}\approx 110\mu H \quad (9)$$

$$L_{m1}=L_{m2}=L_r/k=\frac{110\mu H}{1/5}=550\mu H \quad (10)$$

$$C_{r1}=C_{r2}=\frac{1}{4\pi^2L_rf_r^2}\approx 16nF \quad (11)$$

The voltage stress of S_1-S_8 is equal to $V_{in,max}/2$=400V. MOSFETs IRFP460 with 500V/20A rating are selected for S_1-S_8. The voltage stress and average current of D_1-D_6 are equal to $2(V_o+V_f)=98.2V$ and $I_{o,\max}/4\approx 7.8A$, respectively. Diodes KCU30A30 with 300V/30A rating and 1.1V voltage drop are adopted for D_1-D_4. The adopted capacitances $C_{in1}=C_{in2}$=470μF/450V, $C_{f1}=C_{f2}$=100nF/630V and C_o=2200μF/100V.

V. Experimental Results

The prototype circuit with the circuit components derived in the previous section was tested to demonstrate the performance of the proposed converter. Fig. 6 gives the measured results of the gate voltages, AC terminal voltages resonant inductor currents and resonant capacitor voltages at full load. Two inductor currents and two capacitor voltages are balanced under the test results. Fig. 7 gives the measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at full load. In the same manner, the measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at full load are shown in Fig. 8. Fig. 9 gives the test results of two input capacitor voltages v_{Cin1} and v_{Cin2} and two flying capacitor voltages at full load and 800V input voltage case. It is clear that two input capacitor voltages v_{Cin1} and v_{Cin2} are balanced at 400V and $v_{Cf1}=v_{Cf2}=v_{Cin1}=v_{Cin2}=V_{in}/2$. Fig. 10 shows the measured diode currents and two circuit output currents at full load condition. The output currents i_{o1} and i_{o2} are balanced.

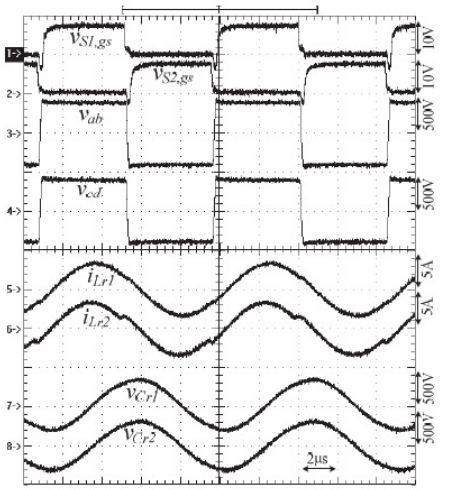


Fig. 6 Measured results of the gate voltages $v_{S1,gs}$ and $v_{S2,gs}$, AC terminal voltages v_{ab} and v_{cd}, resonant inductor currents i_{Lr1} and i_{Lr2}, and resonant capacitor voltages v_{Cr1} and v_{Cr2} at full load.

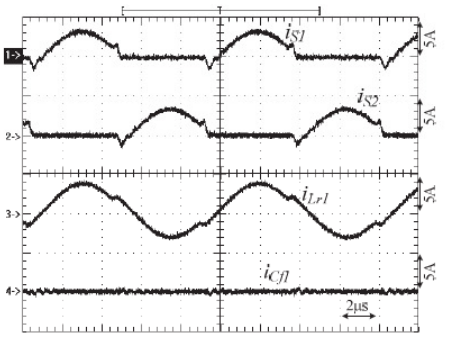


Fig. 7 Measured switch currents i_{S1} and i_{S2}, inductor current i_{Lr1} and flying capacitor current i_{Cf1} at full load.

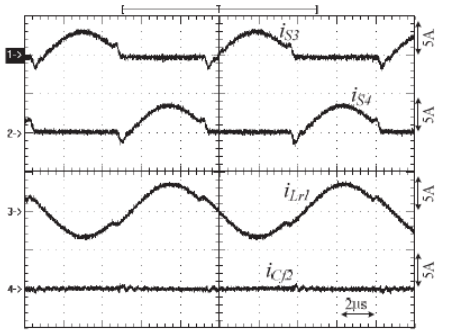


Fig. 8 Measured switch currents i_{S3} and i_{S4}, inductor current i_{Lr1} and flying capacitor current i_{Cf2} at full load.

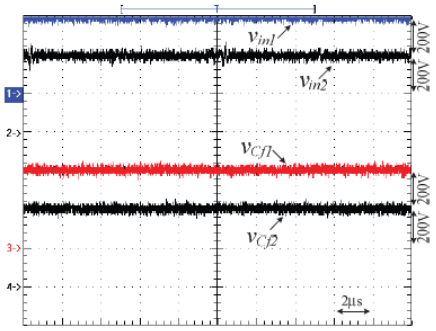


Fig. 9 Measured results of input capacitor voltages and flying capacitor voltages at full load and 800V input voltage case.

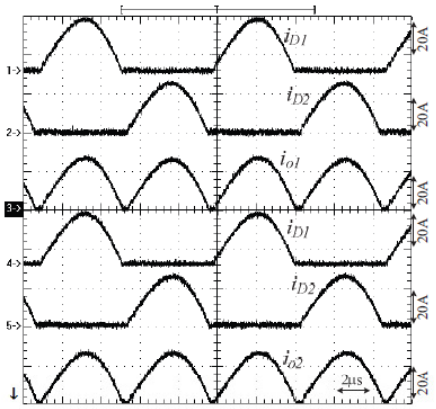


Fig. 10 Measured diode currents and two circuit output currents at full load condition.

VI. Conclusion

This paper presents a new full-bridge resonant converter to have the functions of low voltages stress MOSFETs, ZVS turn-on for MOSFETs, no reverse recovery current on rectifier diodes, the balanced two input capacitor voltages and high circuit efficiency. Two half-bridge converter legs with two spilt capacitors are adopted to reduce the voltage stress of MOSFETs at $V_{in}/2$. Therefore, the proposed converter is suitable used in high input voltage applications. Two flying capacitors C_{f1} and C_{f2} are used to automatically balance two input capacitor voltages in every switching cycle. Two resonant circuits are used to increase the load power and achieve ZVS for all power semiconductors. The system analysis, design example and experiments are presented to demonstrate the effectiveness of the proposed converter.

Acknowledgment

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Asymmetric PWM Converter for High Load Current Application

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***Abstract*—A soft switching converter using low voltage and low current stresses of power components is presented for high input voltage and high output current applications. Two input capacitors and four power MOSFETs are adopted at high voltage side in order to reduce the voltage stress of power switches. Thus, the voltage stress of MOSFETs is clamped at V_{in}/2. Two flying capacitors are adopted at the AC side of two half-bridge converter legs to balance input two capacitor voltages. Three center-tapped rectifiers are used at low voltage side in order to share load current and reduce the size of magnetic core and current stress of passive components. Asymmetric pulse-width modulation is used to generate the gate signals of power MOSFETs and regulate output voltage. Based on the resonant behavior at the transition interval, all power switches can be turned on under zero voltage switching. Finally, experiments are provided to verify the effectiveness of the proposed converter.**

Keywords—PWM converter, ZVS

I. INTRODUCTION

High efficiency power converters have developed and used for portable computer power supplies, telecommunication power units, industry power supplies, data storage systems and server power units. For low power applications, single-stage power converters are normally used in commercial products in order to reduce circuit cost and provide the stable DC output voltage. Two stage power converters are widely used for modern power units. The first stage is a power factor corrector (PFC) based on boost converter to achieve high power factor and reduce line current harmonics. In the second stage DC/DC converter, flyback, forward, half-bridge converter and full-bridge converter are adopted to provide the stable DC output voltage against load current variation. Soft switching techniques such as active clamped circuits [1]-[3], asymmetric pulse-width modulation (PWM) [4]-[5], resonant converters [6]-[8] and phase-shift PWM [9]-[10] have been developed in order to reduce the switching losses and increase circuit efficiency if power converters are operated at high switching frequency. For high voltage application, three-phase AC voltage with power factor correction is adopted in the front stage of AC/DC power converter. The DC bus voltage can be equal to 750V-800V. Thus, the low cost MOSFETs with 500V-650V voltage rating cannot be used in the conventional DC/DC converter such as half-bridge and full bridge converters. Three-level converters [11]-[12] based on neutral-point diode clamp, capacitor clamp or series H-bridge topologies have been proposed to decrease the voltage stress of power devices and increase the switching frequency. Three-level ZVS converters [13]-[14] have been proposed to achieve soft switching for all switches at the desired load range. However, the circuit components and the control scheme are much more complex compared with the conventional DC converters.

A new ZVS converter with low voltage stress MOSFETs and low current stress rectifier diodes is presented for high input voltage and high load current applications. Two split input capacitors and two half-bridge legs are adopted at high voltage side to reduce the voltage stress of MOSFETs at V_{in}/2. Two balance capacitors are adopted between the AC sides of two half-bridge legs in order to balance two split capacitor voltages. For high load current application, three center-tapped rectifiers are used in order to reduce current stress of passive components at low voltage side. Thus, low current stress and small size of passive components can be used at output side. Asymmetric PWM scheme is adopted to generate PWM signals of MOSFETs and regulate output voltage at the desire voltage level. Power MOSFETs can be turned on under ZVS during the transition interval due to the resonant behavior of output capacitance of MOSFETs and leakage inductance. Compared with the conventional parallel three-level converters (with three circuit modules by 12 MOSFETs, 6 clamped diodes, 3 flying capacitors and 3 center-tapped rectifiers), the proposed converter (with 4 MOSFETs, 4 DC blocking capacitors and 3 center-tapped rectifiers) has less circuit components under the same input voltage and output current specifications. The general PWM commercial IC and gate drives are used to generate four gate voltages of MOSFETs. Finally, experiments based on a laboratory prototype were provided to verify the performance of the proposed converter.

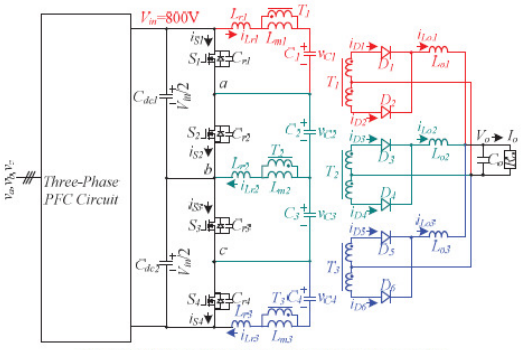

Fig. 1 Circuit configuration of the proposed converter.

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II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

The circuit diagram of the proposed converter is given in Fig. 1. The front stage is a three-phase power factor corrector to achieve the functions of power factor correction and DC bus voltage regulation. The DC bus voltage V_{in} is normally regulated at 750V-800V for three-phase 380/480V AC voltage. Two split capacitors and four power switches are adopted at high voltage side in order to limit the voltage stress of power switches at $V_{in}/2$. To avoid the unbalance input capacitor voltages, two series capacitors C_2 and C_3 are connected in series at AC terminals a and c. When S_1 and S_3 are conducting and S_2 and S_4 are off. The voltage across C_{r2} and C_{r3} is equal to V_{Cdc1}. On the other hand, the voltage across C_{r2} and C_{r3} is equal to V_{Cdc2} if S_2 and S_4 are conducting and S_1 and S_3 are off. Thus, two split capacitor voltages V_{Cdc1} and V_{Cdc2} can be automatically balanced in a switching cycle and $v_{Cdc1}=v_{Cdc2}=v_{C2}+v_{C3}=V_{in}/2$. The DC/DC circuit cells are adopted to reduce the current rating of passive components including diodes, transformers and inductors, share the load current and regulate output voltage at the desire voltage level. The first circuit cell includes C_{dc1}, S_1, S_2, C_{r1}, C_{r2}, L_{r1}, T_1, C_1, D_1, D_2, L_{o1} and C_o. The second circuit cell includes C_{dc1}, C_{dc2}, S_1-S_4, C_{r1}-C_{r4}, C_2, C_3, T_2, L_{r2}, D_3, D_4, L_{o2} and C_o. The third circuit cell includes C_{dc2}, S_3, S_4, C_{r3}, C_{r4}, T_3, L_{r3}, C_4, D_5, D_6, L_{o3} and C_o. V_{in} and V_o are input and output DC bus voltages. C_{dc1} and C_{dc2} are input two capacitors to split input voltage ($V_{Cdc1}=V_{Cdc2}=V_{in}/2$). The voltage stress of each power MOSFET is clamped to $V_{in}/2$. C_{r1}-C_{r4} are the output capacitances of S_1-S_4, respectively. L_{r1}-L_{r3} are the resonant inductances or leakage inductances of T_1-T_3, respectively. L_{m1}-L_{m3} are the magnetizing inductances of T_1-T_3, respectively. T_1-T_3 are the isolation transformers. D_1-D_6 are rectifier diodes. C_1-C_4 are DC blocking capacitances. C_o is output capacitance. The duty cycle control is adopted to generate gate voltages of S_1-S_4 and regulate the output voltage. Due to the resonant behavior by C_{r1}-C_{r4} and L_{r1}-L_{r3}, S_1-S_4 can be turned on under ZVS at the transition interval. Thus, the switching losses of S_1-S_4 are reduced.

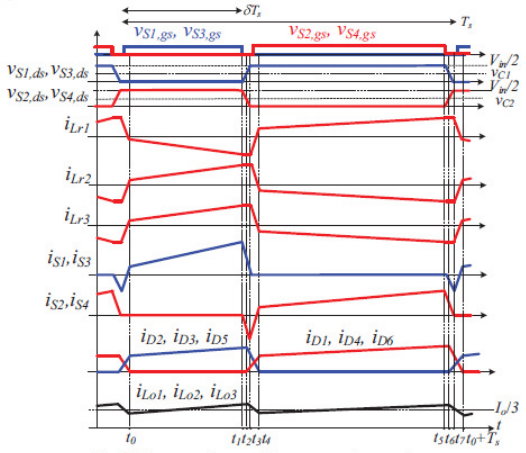


Fig. 2 Key waveforms of the proposed converter.

The operation principle of the proposed converter is based on the following assumptions. Three isolated transformers T_1-T_3 are identical with $L_{m1}=L_{m2}=L_{m3}=L_m$ and turns ratio $n=n_p/n_{s1}=n_p/n_{s2}$. $L_{r1}=L_{r2}=L_{r3}=L_r<<L_m$. $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$. $C_1=C_4=2C_2=2C_3=C_c>>C_r$. $L_{o1}=L_{o2}=L_{o3}=L_o$. Input split capacitances $C_{dc1}=C_{dc2}=C_{dc}$. The key PWM waveforms of the proposed converter in one switching period are shown in Fig. 2. The duty cycle of S_1 and S_3 is δ, and the duty cycle of S_2 and S_4 is 1-δ. Based on the on/off states of S_1-S_4 and D_1-D_6, there are eight operating modes in a switching cycle. The corresponding equivalent circuits of the proposed converter during one switching cycle are given in Fig. 3. Before time t_0, S_1, S_3 and D_1-D_6 are conducting.

Mode 1 [$t_0 \le t < t_1$]: At t_0, $i_{D1}=i_{D4}=i_{D6}=0$ so that D_1, D_4 and D_6 are turned off. The voltage stresses of S_2 and S_4 are equal to V_{Cdc1} and V_{Cdc2}, respectively. The voltage across C_2 and C_3 is equal to V_{Cdc1}. Since $L_m>>L_r$, $v_{Lm1}\approx -v_{C1}$, $v_{Lm2}\approx V_{in}/2-v_{C2}=v_{C3}$ and $v_{Lm3}\approx V_{in}/2-v_{C4}$. The output inductor currents i_{Lo1}-i_{Lo3} increase in this mode. Power is transferred from V_{in} to R_o in this mode. At t_1, power switches S_1 and S_3 are turned off.

Mode 2 [$t_1 \le t < t_2$]: At t_1, S_1 and S_3 are turned off. Since $i_{Lr1}(t_1)<0$, $i_{Lr2}(t_1)>0$ and $i_{Lr3}(t_1)>0$, C_{r1} and C_{r3} are charged and C_{r2} and C_{r4} are discharged in this mode. i_{Lr1}-i_{Lr1} and i_{Lo1}-i_{Lo3} are almost constant in this time interval. At time t_2, $v_{Cr1}=v_{C1}$, $v_{Cr2}=v_{C2}$, $v_{Cr3}=v_{C3}$ and $v_{Cr4}=v_{C4}$.

Mode 3 [$t_2 \le t < t_3$]: At time t_2, $v_{Cr1}=v_{C1}$, $v_{Cr2}=v_{C2}$, $v_{Cr3}=v_{C3}$ and $v_{Cr4}=v_{C4}$. Thus, the primary and secondary winding voltages of T_1-T_3 are all equal to zero voltage. Diodes D_1-D_6 are all conducting so that the output inductor voltages $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. Inductor currents i_{Lo1}-i_{Lo3} all decrease in this mode. i_{D1}, i_{D4} and i_{D6} increase and i_{D2}, i_{D3} and i_{D5} decrease. Since $i_{Lr1}<0$, $i_{Lr2}>0$ and $i_{Lr3}>0$, C_{r1} and C_{r3} are continuously charged and C_{r2} and C_{r4} are discharged in this mode. If the energy stored in L_{r1}-L_{r3} is greater than the energy stored in C_{r1}-C_{r4}, then C_{r2} and C_{r4} can be discharged to zero voltage at time t_3.

Mode 4 [$t_3 \le t < t_4$]: At time t_3, C_{r2} and C_{r4} are discharged to zero voltage. The voltage stress of S_1 and S_3 is clamped at $V_{in}/2$. Since $i_{Lr1}(t_3)<0$, $i_{Lr2}(t_3)>0$ and $i_{Lr3}(t_3)>0$, the anti-parallel diodes of S_2 and S_4 are conducting. S_2 and S_4 can be turned on at this moment to have ZVS operation. In mode 4, D_1-D_6 are all conducting so that $v_{Lr1}=V_{in}/2-v_{C1}$, $v_{Lr2}=-v_{C2}$, $v_{Lr3}=-v_{C4}$ and $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. Thus, i_{Lr1} increases and i_{Lr2}, i_{Lr3} and i_{Lo1}-i_{Lo3} decrease. At time t_4, i_{D2}, i_{D3} and i_{D5} are all decreasing to zero ampere. In this mode, the inductor current variations Δi_{Lr1}-Δi_{Lr3} are equal to $2I_o/(3n)$. In mode 4, S_2 and S_4 are both conducting. However, D_1-D_6 are conducting. Thus, no power is delivered from input voltage to output load. The duty loss in mode 4 is expressed in (1).

$$\delta_{loss,4}=\frac{\Delta t_{34}}{T_s}=\frac{2I_oL_rf_s}{3n(V_{in}/2-v_{C1})}=\frac{2I_oL_rf_s}{3nv_{C2}}=\frac{2I_oL_rf_s}{3nv_{C4}} \quad (1)$$

Mode 5 [$t_4 \le t < t_5$]: At time t_4, i_{D2}, i_{D3} and i_{D5} are all decreasing to zero ampere. Thus, D_2, D_3 and D_5 are off. The voltage stresses of S_1 and S_3 are equal to V_{Cdc1} and V_{Cdc2}, respectively. The voltage across C_2 and C_3 is equal to V_{Cdc2}. In mode 5,

$v_{Lm1}\approx V_{in}/2-v_{C1}$, $v_{Lm2}\approx -v_{C2}$ and $v_{Lm3}\approx -v_{C4}$. The duty cycle δ of S_1 and S_3 is less than 0.5. Based on the voltage-second theorem across the primary side of T_1-T_3, the average capacitor voltages V_{C1} and V_{C3} are greater than $V_{in}/4$ and the average voltages V_{C2} and V_{C4} are less than $V_{in}/4$. Thus, the output inductor current i_{Lo1}-i_{Lo3} decrease in this mode. In this mode, power is transferred from input voltage to output load. At time t_5, S_2 and S_4 are turned off.

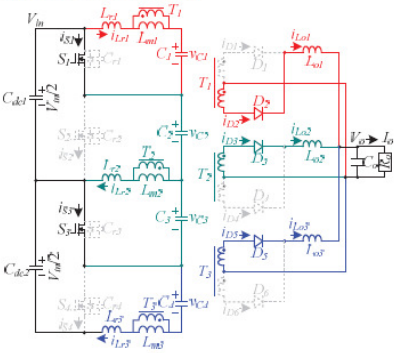
Mode 6 [$t_5 \le t < t_6$]: At t_5, S_2 and S_4 are turned off. Since $i_{Lr1}(t_5)>0$, $i_{Lr2}(t_5)<0$ and $i_{Lr3}(t_5)<0$, C_{r1} and C_{r3} are discharged linearly, and C_{r2} and C_{r4} are charged linearly. In this mode, i_{Lr1}-i_{Lr1} and i_{Lo1}-i_{Lo3} are almost constant. At time t_6, $v_{Cr1}=v_{C1}$, $v_{Cr2}=v_{C2}$, $v_{Cr3}=v_{C3}$ and $v_{Cr4}=v_{C4}$.

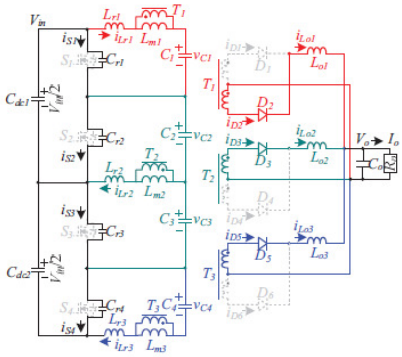
Mode 7 [$t_6 \le t < t_7$]: At time t_6, $v_{Cr1}=v_{C1}$, $v_{Cr2}=v_{C2}$, $v_{Cr3}=v_{C3}$ and $v_{Cr4}=v_{C4}$. Thus, the primary and secondary winding voltages of T_1-T_3 equal zero voltage. Diodes D_1-D_6 are conducting and the output inductor voltages $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. i_{Lo1}-i_{Lo3} all decrease in this mode. i_{D1}, i_{D4} and i_{D6} decrease and i_{D2}, i_{D3} and i_{D5} increase. Since $i_{Lr1}>0$, $i_{Lr2}<0$ and $i_{Lr3}<0$, C_{r1} and C_{r3} are discharged and C_{r2} and C_{r4} are charged. If the energy stored in L_{r1}-L_{r3} is greater than the energy stored in C_{r1}-C_{r4}, then C_{r1} and C_{r3} can be discharged to zero voltage at time t_7.

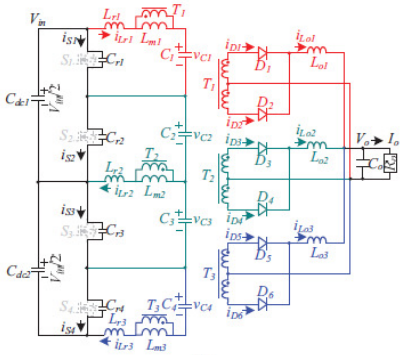
Mode 8 [$t_7 \le t < t_0+T_s$]: At t_7, C_{r1} and C_{r3} are discharged to zero voltage and the voltage stresses of S_2 and S_4 are clamped at v_{Cdc1} and v_{Cdc2}, respectively. Since $i_{Lr1}(t_7)>0$, $i_{Lr2}(t_7)<0$ and $i_{Lr3}(t_7)<0$, the anti-parallel diodes of S_1 and S_3 are conducting. Therefore, S_1 and S_3 can be turned on under ZVS at this moment. In this mode 4, D_1-D_6 are all conducting. Thus, $v_{Lr1}=-v_{C1}$, $v_{Lr2}=v_{C3}$, $v_{Lr3}=V_{in}/2-v_{C4}$ and $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. Inductor currents i_{Lr2} and i_{Lr3} increase, and i_{Lr1} and i_{Lo1}-i_{Lo3} decrease. At time t_0+T_s, i_{D1}, i_{D4} and i_{D6} are all decreasing to zero ampere. In this mode, the inductor current variations Δi_{Lr1}-Δi_{Lr3} are equal to $2I_o/(3n)$. In mode 8, S_1, S_3 and D_1-D_6 are conducting. Thus, no power is delivered from input voltage to output load. The duty loss in mode 8 is expressed in (2).

$$\delta_{loss,8}=\frac{\Delta t_{70}}{T_s}=\frac{2I_oL_rf_s}{3nv_{C1}}=\frac{2I_oL_rf_s}{3n(V_{in}/2-v_{C2})}=\frac{2I_oL_rf_s}{3n(V_{in}/2-v_{C4})} \quad (2)$$

Then the circuit operations of the proposed converter in one switching cycle are completed.


(a)


(b)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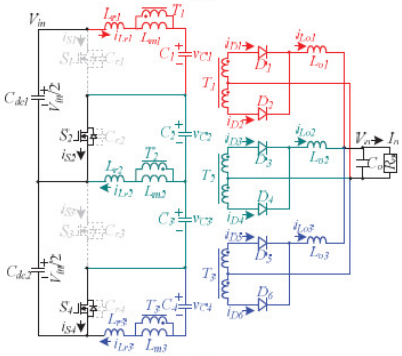
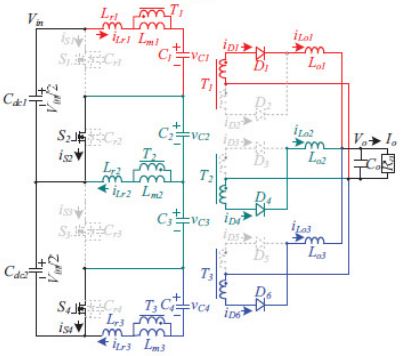

(d)


(e)

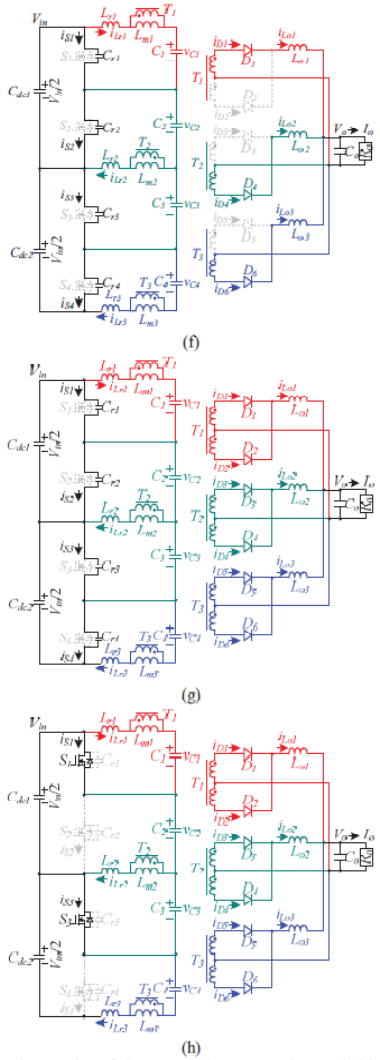


Fig. 3 Operation modes of the proposed converter in a switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8.

III. Circuit Characteristics

Since the charged and discharged times of C_{r1}-C_{r4} in modes 2, 3, 6 and 7 are less than the time interval in the other modes, only modes 1, 4, 5 and 8 are adopted to discuss the circuit characteristics. In steady state, the inductor current variation $\Delta i_{Lr1}=i_{Lr1}(T_s+t_0)-i_{Lr1}(t_0)=0$ and $\Delta i_{Lr2}=\Delta i_{Lr3}=0$. Based on the volt-second balance on (L_{r1} and L_{m1}), (L_{r2} and L_{m2}) and (L_{r3} and L_{m3}), the average capacitor voltages V_{C1}-V_{C4} can be derived as:

$$V_{C1}=V_{C3}=(1-\delta)V_{in}/2 \tag{3}$$

$$V_{C2}=V_{C4}=\delta V_{in}/2 \tag{4}$$

where δ is the duty cycle of S_1 and S_3. From (3) and (4), it can be obtained that $V_{C2}+V_{C3}=V_{in}/2$. In mode 1, $v_{Lo1}=v_{C1}/n-V_o$, $v_{Lo2}=v_{C3}/n-V_o$ and $v_{Lo3}=(V_{in}/2-v_{C4})/n-V_o$. In mode 4, $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. In mode 5, $v_{Lo1}=(V_{in}/2-v_{C1})/n-V_o$, $v_{Lo2}=v_{C2}/n-V_o$ and $v_{Lo3}=v_{C4}/n-V_o$. In mode 8, $v_{Lo1}=v_{Lo2}=v_{Lo3}=-V_o$. Based on the volt-second balance on L_{o1}-L_{o3} at steady state, the DC voltage conversion ratio of the proposed converter is derived as:

$$V_o=\frac{V_{in}}{n}\delta(1-\delta)-\frac{4L_rI_of_s}{3n^2}-V_f \tag{5}$$

where V_f is the voltage drop on each diode of D_1-D_6. From (5), output voltage V_o is related to duty cycle δ, input voltage V_{in}, switching frequency f_s, resonant inductance L_r, turns ratio n and load current I_o. The average magnetizing currents of L_{m1}-L_{m3} can be obtained by the current-second balance on DC blocking capacitances C_1-C_4.

$$I_{Lm1}=\frac{(2\delta-1)I_o}{3n},\ I_{Lm2}=I_{Lm3}=\frac{(1-2\delta)I_o}{3n} \tag{6}$$

The ripple currents on inductances L_{m1}-L_{m3} can be expressed as:

$$\Delta i_{Lm}=\frac{V_{C1}(\delta-\delta_{loss,8})T_s}{L_m}=\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{2L_m} \tag{7}$$

From (6)-(8), the maximum and minimum magnetizing currents of L_{m1}-L_{m3} can be obtained in (9)-(12).

$$i_{Lm1,\max}=\frac{(2\delta-1)I_o}{3n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m} \tag{8}$$

$$i_{Lm2,\max}=i_{Lm3,\max}=\frac{(1-2\delta)I_o}{3n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m} \tag{9}$$

$$i_{Lm1,\min}=\frac{(2\delta-1)I_o}{3n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m} \tag{10}$$

$$i_{Lm2,\min}=i_{Lm3,\min}=\frac{(1-2\delta)I_o}{3n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m} \tag{11}$$

The ripple current of L_{o1}-L_{o3} can be expressed in (12).

$$\begin{aligned}\Delta i_{Lo}&=\frac{[V_{C1}/n-V_o-V_f](\delta-\delta_{loss,8})T_s}{L_o}\\&=\frac{[\frac{(1-\delta)(1-2\delta)V_{in}}{2n}+\frac{4L_rI_of_s}{3n^2}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})T_s}{L_o}\end{aligned} \tag{12}$$

The maximum and minimum output inductor currents are expressed as:

$$\begin{aligned}i_{Lo1,\max}=i_{Lo2,\max}=i_{Lo3,\max}&=\frac{I_o}{3}+[\frac{(1-\delta)(1-2\delta)V_{in}}{2n}\\&+\frac{4L_rI_of_s}{3n^2}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \tag{13}$$

$$\begin{aligned}i_{Lo1,\min}=i_{Lo2,\min}=i_{Lo3,\min}&=\frac{I_o}{3}-[\frac{(1-\delta)(1-2\delta)V_{in}}{2n}\\&+\frac{4L_rI_of_s}{3n^2}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \tag{14}$$

The average diode currents are given as:

$$I_{D1}=I_{D4}=I_{D6}\approx(1-\delta)I_o/3,\ I_{D2}=I_{D3}=I_{D5}\approx\delta I_o/3 \quad (15)$$

The voltage stresses of diodes D_1-D_6 are expressed as:

$$V_{D1,stress}=V_{D4,stress}=V_{D6,stress}\approx\frac{2V_{C1}}{n}=\frac{(1-\delta)V_{in}}{n} \quad (16)$$

$$V_{D2,stress}=V_{D3,stress}=V_{D5,stress}\approx\frac{2(V_{in}/2-V_{C1})}{n}=\frac{\delta V_{in}}{n} \quad (17)$$

The root-mean-square (rms) currents of S_1-S_4 can be obtained as:

$$i_{S1,rms}=i_{S3,rms}\approx\frac{(1-\delta)I_o}{n}\sqrt{\delta},\ i_{S2,rms}=i_{S4,rms}\approx\frac{\delta I_o}{n}\sqrt{1-\delta} \quad (18)$$

The voltage stresses of S_1-S_4 are equal to $V_{in}/2$. At time t_1, the inductor currents i_{Lr1}-i_{Lr3} are approximately expressed as:

$$\begin{aligned}i_{Lr1}(t_1)&\approx i_{Lm1,\min}-\frac{i_{Lo1,\max}}{n}\\&\approx\frac{(2\delta-1)I_o}{3n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m}-\frac{I_o}{3n}\\&-[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{3n^3}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \quad (19)$$

$$\begin{aligned}i_{Lr3}(t_1)=i_{Lr2}(t_1)&\approx i_{Lm2,\max}+\frac{i_{Lo2,\max}}{n}\\&\approx\frac{(1-2\delta)I_o}{3n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m}+\frac{I_o}{3n}\\&+[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{3n^3}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \quad (20)$$

At t_5, the inductor currents i_{Lr1}-i_{Lr3} are approximately given as:

$$\begin{aligned}i_{Lr1}(t_1)&\approx i_{Lm1,\max}+\frac{i_{Lo1,\min}}{n}\\&\approx\frac{(2\delta-1)I_o}{3n}+\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m}+\frac{I_o}{3n}\\&-[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{3n^3}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \quad (21)$$

$$\begin{aligned}i_{Lr3}(t_5)=i_{Lr2}(t_5)&\approx i_{Lm2,\min}-\frac{i_{Lo2,\min}}{n}\\&\approx\frac{(1-2\delta)I_o}{3n}-\frac{\delta(1-\delta)V_{in}T_s-4L_rI_o/(3n)}{4L_m}-\frac{I_o}{3n}\\&+[\frac{(1-\delta)(1-2\delta)V_{in}}{2n^2}+\frac{4L_rI_of_s}{3n^3}](\delta-\frac{4L_rI_of_s}{3nV_{in}(1-\delta)})\frac{T_s}{2L_o}\end{aligned} \quad (22)$$

If the energy stored in L_{r1}-L_{r3} at time t_1 is greater than the energy stored in C_{r1}-C_{r4} in modes 2 and 3, then C_{r2} and C_{r4} can be discharged to zero voltage. The ZVS condition of S_2 and S_4 can be given as:

$$L_r\geq\frac{C_rV_{in}^2}{i_{Lr1}^2(t_1)+i_{Lr2}^2(t_1)+i_{Lr3}^2(t_1)} \quad (23)$$

If the energy stored in L_{r1}-L_{r3} at time t_5 is greater than the energy stored in C_{r1}-C_{r4} in modes 6 and 7, then C_{r1} and C_{r3} can be discharged to zero voltage. The ZVS condition of S_1 and S_3 can be given as:

$$L_r\geq\frac{C_rV_{in}^2}{i_{Lr1}^2(t_5)+i_{Lr2}^2(t_5)+i_{Lr3}^2(t_5)} \quad (24)$$

The necessary resonant inductance L_r can be obtained in (25) to achieve ZVS turn-on for S_1-S_4.

$$L_r\geq\max\{\frac{C_rV_{in}^2}{i_{Lr1}^2(t_1)+i_{Lr2}^2(t_1)+i_{Lr3}^2(t_1)},\frac{C_rV_{in}^2}{i_{Lr1}^2(t_5)+i_{Lr2}^2(t_5)+i_{Lr3}^2(t_5)}\} \quad (25)$$

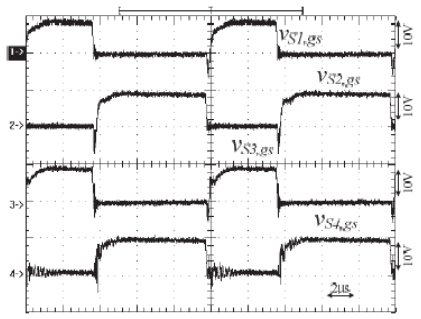


Fig. 4 Measured results of PWM waveforms of S_1-S_4 at full load and V_{in}=800V.

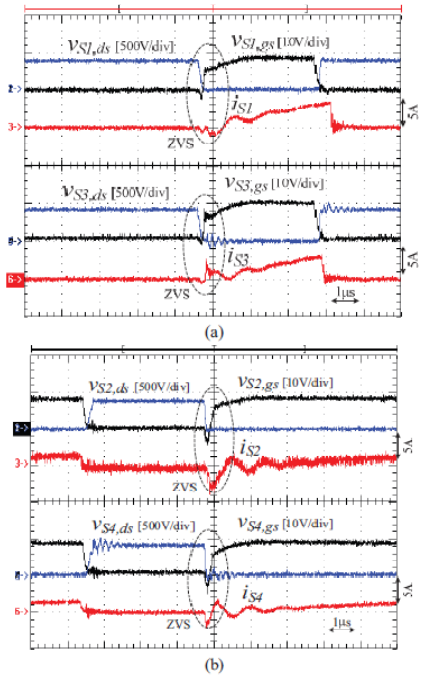


Fig. 5 Measured waveforms of gate voltages, drain voltages and switch currents at 25% load and V_{in}=800V (a) S_1 and S_3 (b) S_2 and S_4.

IV. Experimental Results

Experiments based on a laboratory prototype are presented in this section to verify the effectiveness of the proposed converter. The electrical specifications of the converter are V_{in}=750 – 800V, V_o=24V, I_o=60A and f_s=100kHz. The circuit

parameters of the prototype are C_{dc1}=C_{dc2}=330μF, S_1-S_4: IRFP460, D_1-D_6: 30CPQ150, L_{r1}-L_{r3}: 16μH,, C_1=C_4=100μH, C_2=C_3=50μH, L_{m1}=L_{m2}=L_{m3}=0.5mH, n_{T1}-n_{T3}: 33:5:5, L_{o1}-L_{o3}: 10μH and C_o=4400μF. The measured PWM waveforms of S_1-S_4 at full load with different input voltage are shown in Fig. 4. Fig. 5 gives the experimental results of gate voltage, drain voltage and switch current of S_1-S_4 at 25% load. Before S_1-S_4 are turned on, drain currents are negative to discharge the drain-to-source capacitors. Therefore, S_1-S_4 can be turned on under ZVS when drain voltages are decreased to zero voltage. The experimental waveforms of two input capacitor voltages v_{Cdc1} and v_{Cdc2} and capacitor voltage v_{C2}+v_{C3} at full load and 800V input voltage are shown in Fig. 6. Two input capacitor voltages v_{Cdc1} and v_{Cdc2} are balanced at 400V and v_{C2}+v_{C3}=v_{Cdc1}=v_{Cdc2}=400V. Fig. 7 shows the measured waveforms of the output inductor currents i_{Lo1}, i_{Lo2}, i_{Lo3} and i_{Lo1}+i_{Lo2}+i_{Lo3} at full load condition.

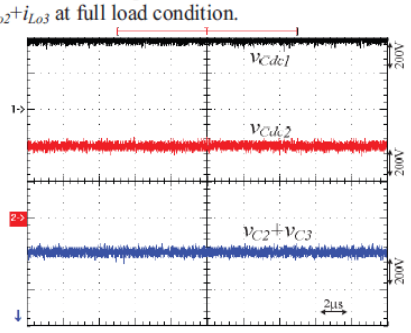


Fig. 6 Measured results of input capacitor voltages v_{Cin1} and v_{Cin2} and capacitor voltage v_{C2}+v_{C3} at full load and V_{in}=800V.

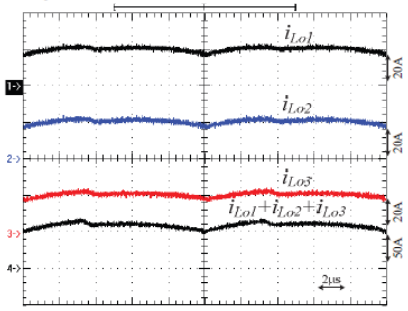


Fig. 7 Measured waveforms of output inductor currents i_{Lo1}, i_{Lo2}, i_{Lo3} and i_{Lo1}+i_{Lo2}+i_{Lo3} at full load.

V. Conclusion

A new PWM converter for high voltage and high load current applications is presented in this paper to reduce the voltage stress of power devices at the high voltage side and decrease the current stress of passive components at low voltage side. Low voltage rating of MOSFETs and low current stress of passive components can be adopted in the proposed converter to meet the size and high switching frequency demand. Two half-bridge converter legs with two spilt capacitors are used at high voltage side to clamp the voltage stress of MOSFETs at V_{in}/2. Two DC or flying capacitors C_2 and C_3 are connected at the AC terminal of two converter legs in order to balance two input split capacitor voltages. Three ZVS DC circuits are connected in series at high voltage side and connected in parallel at low voltage side to reduce the size and current rating of passive components at the secondary side. Compared to the conventional parallel three-level converter, the proposed converter has less power switch counts. Finally, experiments are provided to verify the effectiveness of the converter.

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