出國報告 (出國類別: 國際會議)

# 出席 IEEE 2014 國際射頻及無線研討會

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派赴國家：美國

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## 摘要

感謝學校的補助與支持，學生本次得以參加 2014 國際射頻及無線研討會(IEEE 2014 Radio and Rireless Symposium)，該會議於 1 月 19 至 22 日在美國加州 Newport Beach 舉行。該會議是串連其它幾個會議(RAWR、WiSNet、BioWireleSS、SiRF)，由微波理論與技術學會(IEEE MTT-S)所主辦，形成 IEEE 微波界的無線通訊週(Radio Wireless Week)。本次學生出國目的為於該會議進行口頭論文發表，並於會場參與聆聽其它主題之演講。這次是學生首度參加國際射頻及無線研討會，在此次會議中，除了增進個人專業領域的國際視野外，在英語能力方面也有些地進步，但同時也更深切地了解到英語的重要性。另外於此會議，在這短短幾天中，也使我有機會從其他來自世界各國的優秀研究學者身上學習，觀察他們研究問題與處理問題的思維方式及對研究的熱忱與態度，這些對我往後的研究方向及人生規劃有相當大的啟發。希望以後能夠繼續參與各重要之國際學術研討會，最後學生感謝學校補助使學生得以出席今年的國際射頻及無線研討會。

[ 2014 Radio and Rireless Symposium website：hhttp://www.radiowirelessweek.org/2014/ ]

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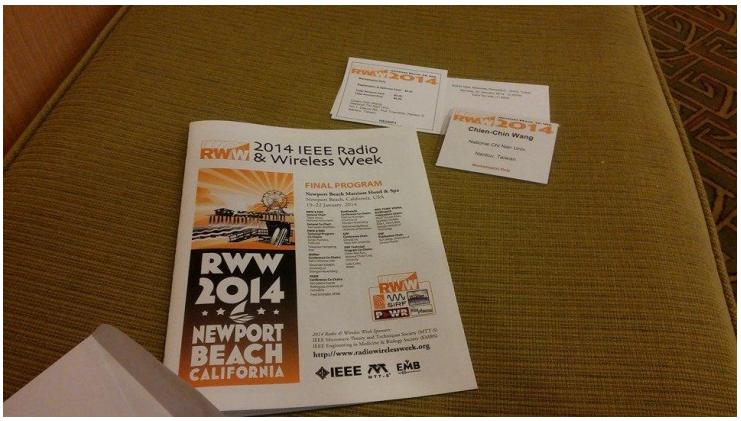
## 一、會議目的

今年 2014 的國際射頻及無線研討會(IEEE Radio and Rireless Symposium)於 1 月 19 至 22 日在美國加州 Newport Beach 舉行。該會議是串連其它幾個會議(RAWR、WiSNet、BioWireleSS、SiRF)一同舉辦，形成 IEEE 微波界的無線通訊週(Radio Wireless Week)，其大會衷旨乃致力於無線通訊理論、系統、電路及元件等不同領域的技術或應用整合，提供一個學術論壇的交流平台，使來自不同研究領域的專家學者能夠針對最前瞻尖端無線系統及終端應用之各種技術一起共同討論，相互激發想法。該會議以彌補數位、射頻、硬體及軟體等技術領域間的縫隙為目標，期盼達到無縫接軌，以促進無線產業及行動應用的成長。本次學生出國目的為於該會議進行口頭論文發表，並於會場參與聆聽其它主題之演講。

## 二、會議過程

學生搭乘華航自臺北往洛杉磯的直航班機，於當地時間 19 日中午 12:40 抵達洛杉磯國際機場，接著再由接駁巴士到達 Newport Beach 旅館辦理入住事宜。隔日中午，學生便前往會場辦理註冊並取得會議相關資料(如附圖一)，接著到當天下午要進行口頭簡報的場地確認(如附圖二)，隨後便先前往會場供餐地點用餐並利用時間準備待會口頭報告。

下午 3:40 學生出席所指定場次進行論文發表，此場次主題為”Advanced Transceiver Technologies”，主持人是來自 OmniVision Technologies,Inc.的 Dr. Xin Wang，Speaker 共四位，每位報告時間共 20 分鐘。學生發表之論文題目為”A 21.1 mW 6.2 dB NF 77~81 GHz CMOS Low-Noise Amplifier with 13.5±0.5 dB $S_{21}$ and Excellent Input and Output Matching for Automotive Radars”。 近年來，由於矽 IC 製程技術的快速進展，以其實現高度整合且低成本的毫米波系統(例如 71~76 GHz 及 81~86 GHz 高速點對點連結、76~77 GHz 長距離及 77~81 GHz 短距離汽車雷達)逐漸成為目前熱門的研究領域。在收發機中，低雜訊放大器為相當重要的前




附圖一 會場辦理註冊所取得會議相關資料


附圖二 學生於進行論文口頭發表之指定場次前留影


附圖三 Panel session:“兆赫波影像:看見的與看不見的”之會場情況

端電路，為相當重要的前端電路，其必須在低訊雜比下將天線接收到的微弱 RF 訊號放大。此 LNA 的基本要求包括:良好輸出/輸入匹配、高隔離度、高增益、低雜訊及低功率損耗。然而，查考近年相關文獻，絕大多數的 77Gz LNA 皆以 SiGe bipolar 製程技術設計/實現，很難同時達到以上要求，特別是增益與功率損耗，兩者往往不能兼備。在本論文中，我們提出一有效增加增益頻寬($S_{21}$)的設計方法，電路由三級 common source 組態所構成，每級輸出皆採用低品質因子 RLC 諧振腔，而藉由調整該三級諧振腔的頻率(低角頻率、中角頻率、高角頻率)拉大 3dB 增益頻寬。另外，本電路採用了成本相較 SiGe bipolar 便宜的 CMOS 90 nm 技術來設計，該技術除了 low cost 外同時具低功耗特點。從晶片量測結果來看，本電路在 77~81GHz 操作頻率下，功率損耗僅為 21.1mW，但增益($S_{21}$)達到 13.5±0.5dB，在雜訊指數表現方面，則只有 6.2dB，結果顯示，本 77Gz LNA 電路與先前文獻相比，在低功率損耗操作下仍然有極優異的性能表現，非常適合於毫米波通訊系統應用。當口頭報告結束後，在場有一位女教授提問，好奇我們是如何設計電路中的傳輸線電感及如何做佈局後模擬，使電路能相當準確設計在 W-頻帶極高頻應用上，在當時誠實說相當考驗我英文對答能力，我希望能盡量清楚地答覆她的問題。我的回答是我們主要利用 TSMC 晶圓廠提供的 90nm 製程的環境參數搭配 SONET 電磁模擬軟體來建立 W-頻帶傳輸線的資料庫。由於一般 TSMC 所提供的元件模型只準確至 30GHz，為了符合操作頻率 30GHz 以上的應用，我們先作 90nm 製程環境參數校正，該製程的介電層與導電層參數值通常具有一定誤差範圍，詳細誤差值可由製程文件資料得到，接著再由 SONET 軟體去模擬內建元件，藉由調整 EM 模擬的環境參數去 fit 出與內建元件 raw data 近似的 S 參數，進而得到較為精確的 EM 模擬環境，之後便可利用該環境設計傳輸線及做電路整體後佈局模擬。該 session 結束後，在場許多學者均對我們傳輸線設計方法相當感興趣，詢問了許多相關設計細節問題，並同時對於我們電路設計與布局考量提出許多寶貴的建議，大家也都彼此交換意見，收穫良多。

隔日中午 12 點，學生參與聆聽一場 Panel session(如附圖三)，被邀請來的演講者為來自美國 NASA Jet Propulsion Laboratory 同時也是 IEEE Fellow 的 Dr. Peter H. Siegel，其談論的主題為”兆赫波影像:看見的與看不見的”(THz Imaging: What You See and What you Don’t)，兆赫波(THz)對於科學技術研究來說，這是一塊尚待開發的新領域，該頻帶介於 300GHz 至 3000GHz，高於傳統電子的微波頻率但低於光與紅外線的區域。許多國防科技研究組織已驗證 THz 感測及影像技術，然而，近年來世界各地許多 CMOS 前瞻技術及固態電路的研究學者紛紛投入於未來將做為商業用途的 THz 通訊系統之研究。標準制定組織也已開始參與制定 THz 通訊標準，然而 THz 通訊的研究開發極具挑戰性，除了需要 THz 訊號源外，適合的接收機系統架構、OTA 測試、深入了解材料及環境的電磁傳播及吸收/幅射特性等，以上皆為不可或缺的條件。同時，投入研發的資金成本與時間、昂貴硬體的開發及測試方法，也使得商業應用 THz 技術之實現備受挑戰。此 Panel session 即在探討 THz 通訊技術未來發展的挑戰與前景。下午 4:00PM 接著參加 TU5B:Lated News 場次，主持人為來自美國 MIT Lincoln Laboratory 的 Dr. Kevin Chuang，論文討論之內容，包括: (1)應用於無線區域網路之 5-5.8GHz CMOS 單晶功率放大器(A 5-5.8 GHz Fully-Integrated CMOS PA for WLAN Applications) ， 提報 人 為 J. Tsai(National Taiwan Normal University, Taipei, Taiwan)，其提出一新的 PA 電路架構並以 CMOS 技術設計實現晶片，解決以往 SiGe 技術成本過高的問題。(2) 利用峰波因數抑制及數位預失真技術之前瞻性發送機(Advanced Transmitters with Combined Crest Factor Reduction and Digital Predistortion Techniques)，提報人為 A. Farabegoli (Intel Mobile Communication GmbH, Neubiberg, Germany)，其提出之發射機電路使用峰波因數抑制及數位預失真技術以達到極佳的功率效率。(3)應用於具延伸性峰值功率比寬頻訊號有效放大之三路 Doherty 功率放大器 (Three-Way Doherty Power Amplifier for Efficient Amplification of Wideband Signals with Extended PAPR)，提報人為 H. Golestaneh (University of Waterloo,

Waterloo, Canada)，其利用 Doherty 功率放大器本身特性優點及功率 divide/combine 三條路徑來達成高線性度和高效率的目標。

學生此次國際學術會議之行，不僅讓我更明白國際學術會議在學術研究發展上所扮演之角色，同時也擴展我的人生視野，使我有機會從其他來自世界各國的優秀研究學者身上學習，觀察他們研究問題與處理問題的思維方式及對研究的熱忱與態度，這些對我往後的研究方向及人生規劃有相當大的啟發。順利完成此學術會議之工作後，學生於 1 月 26 日從洛杉磯國際機場搭乘華航直飛臺北的班機回國，於臺北時間 1 月 27 日 9:10 抵達桃園機場。

## 三、心得及建議事項

此次是學生首度參加國際射頻及無線研討會(IEEE Radio and Rireless Symposium)，與會人士眾多，射頻與無線通訊相關領域之專家學者來自世界各地，並看到有許多國際知名大廠來此設立攤位，展示其最先進的產品及技術，並與現場與會人士交流熱絡。此行除了增進個人專業領域的國際視野外，在英語能力方面也有些地進步，但同時也更深切地了解到英語的重要性，特別是對國內工科系學生來說(包括自己在內)，應要加強英文口語表達能力，這對於往後參與國際學術研究或是在國際學術場合上都會有很大的幫助。此次國際性大型學術研討會之行，不僅可以了解世界上相關領域的研究方向以及研究深度之外，並且能提升研究水準與拓展國際視野，因此有志於長期研究的學者或是研究生更應鼓勵多參與國際性的研討會，藉由和與會的學者互相討論也可以激發出不錯的研究想法。所以，若能夠持續在經費上得到國科會的適當補助，對於研究學者或是研究生將會有極大的幫助。

## 四、攜回資料名稱及內容

無

## 五、附件

發表論文

# A 21.1 mW 6.2 dB NF 77~81 GHz CMOS Low-Noise Amplifier with 13.5±0.5 dB $S_{21}$ and Excellent Input and Output Matching for Automotive Radars

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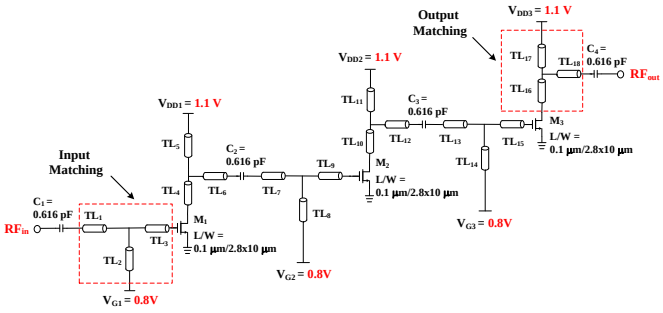
***Abstract*** **— A low power and wideband three-stage millimeter-wave (MMW) low-noise amplifier (LNA) using standard 90 nm CMOS technology is reported. T-network (or π-match) is utilized to achieve simultaneously wideband input and output impedance matching, wideband power gain ($S_{21}$) and wideband NF at W-band. The LNA consumes 21.1 mW, achieving $S_{11}$ better than −10 dB for frequencies 62.3~82.4 GHz, $S_{22}$ better than −10 dB for frequencies 62.8~84.6 GHz, $S_{12}$ better than −29 dB for frequencies 72~84 GHz, and group delay variation smaller than ±6.5 ps for frequencies 70~90 GHz. Additionally, high and flat $S_{21}$ of 13.1±1.5 dB is achieved for frequencies 72~84 GHz, which means the corresponding 3-dB bandwidth is 12 GHz. Furthermore, the LNA achieves minimum noise figure (NF) of 6.2 dB at 78 GHz and NF of 6.8±0.6 dB for frequencies 75~82 GHz, one of the best NF results ever reported for a W-band CMOS LNA.**

***Index Terms*** **— LNA, CMOS, low power, W-band, automotive radar.**

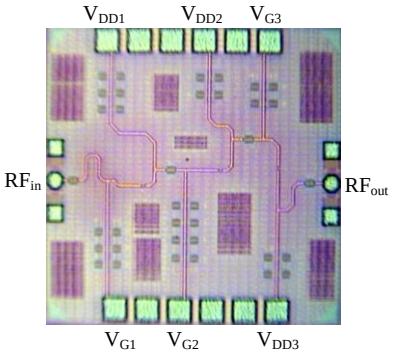
## I. INTRODUCTION

Recently, thanks to the rapid development of CMOS/ BiCMOS processes, it has become possible to use them to implement MMW communication systems for 71~76 GHz high-speed point-to-point wireless link, 76~77 GHz long range automotive radar and 77~81 GHz short range automotive radar. In transceiver design, LNA is a critical block, which receives small RF signals from antenna over the whole band of interest and then amplifies them with a good SNR property. The basic requirements of an LNA include good input and output impedance matching ($S_{11}$ and $S_{22}$), high reverse isolation ($S_{12}$), high forward gain ($S_{21}$), low NF and high power linearity (or phase linearity), and low power consumption ($P_{DC}$).

Recently, several excellent W-band CMOS/BiCMOS LNAs have been reported [1]-[4]. However, the overall performances of these W-band LNAs are not satisfactory. For example, in [2], a two-stage 77~81 GHz LNA in 0.18 μm SiGe BiCMOS process was demonstrated. Though high and flat $S_{21}$ of 13.8±0.7 dB and low NF of 6.9 dB were achieved, its $P_{DC}$ of 37 mW was not good enough. In the current work, the purpose is to demonstrate that low $P_{DC}$ (< 25 mW), high $S_{21}$ (> 10 dB), low NF (< 7 dB) and excellent phase linearity (i.e. group delay variation smaller than ±8 ps) can be achieved simultaneously for a wideband LNA that is suitable for commercial 71~76 GHz, 76~77 GHz, and 77~81 GHz bands by using a relatively cost-effective 90 nm CMOS technology.




(a)

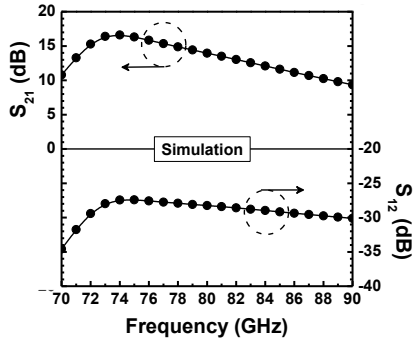



(b)

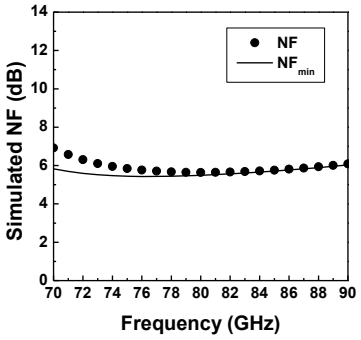
Fig. 1 (a) Schematic diagram, and (b) chip micrograph of the W-band CMOS LNA.

## II. CIRCUIT DESIGN

Fig. 1(a) shows the schematic diagram of the W-band CMOS LNA with important device parameters labeled. It constitutes three common-source (CS) stages. To maximize the 3 dB bandwidth of $S_{21}$, the output of each stage was equivalently loaded with a low-Q RLC parallel resonant circuit. Over the W-band of interest, the load resonant




(a)




(b)

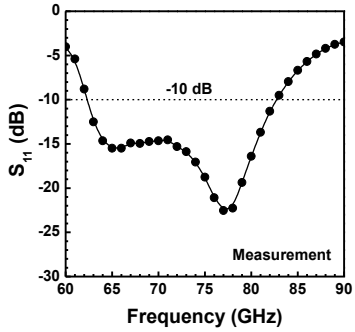
Fig. 2 Simulated (a) $S_{21}$ and $S_{12}$, and (b) NF and $NF_{min}$ versus frequency characteristics of the W-band LNA.

frequency of the first, second, and third stage are close to the lower corner frequency, center frequency, and upper corner frequency, respectively. Based on the methodology in [5]-[6], simultaneous input impedance and noise matching over the W-band of interest were achieved by appropriately selecting the values of $TL_1$~$TL_{18}$ as well as the size and bias of the input transistor $M_1$, i.e. $C_{gs1}$ and $g_{m1}$.

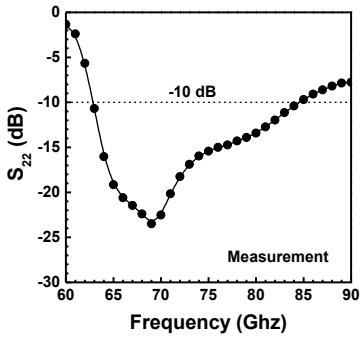
Fig. 2(a) shows the simulated $S_{12}$ and $S_{21}$ versus frequency characteristics of the W-band LNA. High and flat $S_{21}$ of 14±1.5 dB is achieved for frequencies 76.7~83.1 GHz. That is, the corresponding 3-dB bandwidth of $S_{21}$ is 6.7 GHz. In addition, the LNA achieves $S_{12}$ better than −27.8 dB for frequencies 76.7~83.1 GHz. Fig. 2(b) shows the simulated NF and $NF_{min}$ versus frequency characteristics of the W-band LNA. The LNA achieves minimum NF of 5.64 dB at 80 GHz and NF of 5.74±0.1 dB for frequencies 75~86 GHz, an excellent result for a W-band CMOS LNA.

## III. MEASUREMENT RESULTS AND DISCUSSIONS

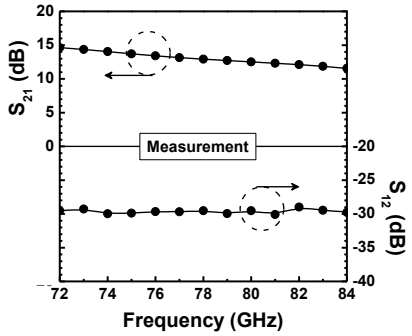
The chip micrograph of the finished circuit is shown in Fig. 1(b). The chip area is 740×800 μm$^2$ excluding the test pads. On-wafer S-parameters and NF measurements were performed by an Agilent E7350A network analyzer and Agilent E5052A NF analyzer, respectively. The LNA was biased in the condition of $V_{DD1} = V_{DD2} = V_{DD3} = 1.1$ V, $V_{G1} = V_{G2} = V_{G3} = 0.8$ V, and $I_{d1} = I_{d2} = I_{d3} = 6.4$ mA. That is, the




(a)




(b)




(c)

Fig. 3 Measured (a) $S_{11}$, (b) $S_{22}$, and (c) $S_{21}$ and $S_{12}$ versus frequency characteristics of the W-band LNA.

power consumption of the LNA is 21.1 mW, a relatively low value for a W-band CMOS LNA.

Fig. 3(a) shows the measured $S_{11}$ versus frequency characteristics of the W-band LNA. The LNA achieves minimum $S_{11}$ of −22.5 dB at 77 GHz, and $S_{11}$ better than −10 dB for frequencies of 62.3~82.4 GHz. Fig. 3(b) shows the measured $S_{22}$ versus frequency characteristics of the W-band LNA. The LNA achieves minimum $S_{22}$ of −23.5 dB at 69 GHz, and $S_{22}$ better than −10 dB for frequencies of 62.8~84.6 GHz. Fig. 3(c) shows the measured $S_{12}$ and $S_{21}$ versus frequency characteristics of the W-band LNA. The LNA achieves $S_{12}$ better than −29 dB for frequencies 72~84 GHz. Additionally, high and flat $S_{21}$ of 13.1±1.5 dB is achieved for frequencies 72~84 GHz, which means the corresponding 3-dB bandwidth is 12 GHz.

Fig. 4 shows the measured NF versus frequency characteristics of the W-band LNA. The LNA achieves

Table I Summary of the implemented W-band CMOS LNA, and recently reported state-of-the-art W-band CMOS and SiGe BiCMOS LNAs.

| | Frequency (GHz) | BW (GHz) | $S_{11}$ (dB) | $S_{22}$ (dB) | $S_{21}$ (dB) | NF (dB) | P1dB (dBm) | IIP3 (dBm) | $P_{DC}$ (mW) | FOM (GHz/mW) | Technology |
|---|---|---|---|---|---|---|---|---|---|---|---|
| This Work | 77~81 | 12 | <-13 | <-12 | 13±0.5 | 6.2 | -20 | -11 | 21.1 | 0.8 | 90 nm CMOS |
| [1] 2011 NEWCAS | 77~81 | 6.5 | <-10 | <-13 | 8.5±1.5 | 7.2 (Simulation) | -18 | NA | 9 | 0.45 | 0.13 mm SiGe BiCMOS |
| [2] 2010 MWCL | 77~81 | 14 | <-11 | <-17 | 13.5±1 | 7 | -11.4 | NA | 37 | 0.44 | 0.18 mm SiGe BiCMOS |
| [3] 2012 IEEE RFIT | 76~77 | 7 | -10 | -5 | 11 | 7.8 | -40 | NA | 25.8 | 0.19 | 65 nm CMOS |
| [4] 2012 MWCL | 66~78 | 12 | <-5 | <-7 | 21.3 | 7.6 | -18 (Simulation) | NA | 40 | 0.73 | 0.25 mm SiGe BiCMOS |

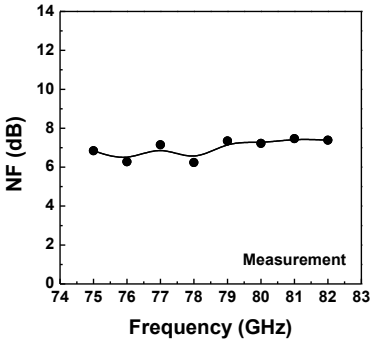


Fig. 4 Measured NF versus frequency characteristics of the W-band LNA.

minimum NF of 6.2 dB at 78 GHz and NF of 6.8±0.6 dB for frequencies 75~82 GHz, one of the best NF results ever reported for a W-band CMOS LNA. In addition, the measured group delay variation was only ±6.5 ps for frequencies 70~90 GHz, an excellent result for a W-band CMOS LNA (not shown here). The LNA was unconditionally stable for frequencies 50~100 GHz (not shown here). At 79 GHz, the measured $P_{1dB}$ and IIP3 are –20 dBm and –11 dBm, respectively (not shown here).

A figure of merit (FOM) suitable for evaluating the performance of wideband LNAs can be defined as below:

$$\text{FOM [GHz/mW]} = \frac{S_{21}[1]\cdot \text{BW[GHz]}}{(\text{NF}-1)[1]\cdot P_{DC}[\text{mW}]}, \quad (1)$$

where $S_{21}[1]$ represents the average power gain in magnitude; BW[GHz] represents the 3 dB-bandwidth in GHz; (NF-1)[1] represents the excess NF in magnitude; and $P_{DC}$[mW] represents power dissipation in mW. This FOM includes the most relevant parameters for evaluating LNAs for low-power, high-gain, low-noise, and wideband applications. Table I is a summary of the implemented W-band CMOS LNA, and recently reported state-of-the-art W-band CMOS or SiGe BiCMOS LNAs in [1]-[4]. Compared with other work, our LNA exhibits not only low $P_{DC}$ but one of the lowest NFs and highest FOMs. The results indicate that the proposed LNA architecture is promising for W-band communication systems.

## IV. CONCLUSIONS

In this work, we demonstrate a low power and low NF W-band LNA using 90 nm CMOS technology. The LNA comprises three CS stages. The LNA consumes 21.1 mW, achieving group delay variation smaller than ±6.5 ps for frequencies 70~90 GHz, and high and flat $S_{21}$ of 13.1±1.5 dB for frequencies 72~84 GHz. In addition, the LNA achieves minimum NF of 6.2 dB at 78 GHz and NF of 6.8±0.6 dB for frequencies 75~82 GHz, one of the best NF results ever reported for a W-band CMOS or SiGe BiCMOS LNA. The results from this work indicate the high potential of the proposed LNA in W-band transceiver applications.

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