出國報告（出國類別：其他-國際會議）

參加「二〇一四年IEEE ICIT國際學術研討會」出國報告

服務機關：國立雲林科技大學電機系
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派赴國家：韓國
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出國期間：103 年 2 月 27 日至 103 年 3 月 2 日

摘要

出席二〇一四年 IEEE-ICIT 國際會議，此行之主要目的是向國際電力電子專家學者介紹國內電力電子之研究成果、並且學習國外電源轉換技術，與專家學者共同討論高效率電源轉換器術與再生能源之應用與研究趨勢。聆聽各國學者與業界工程師在電力電子技術、能源控制、智慧控制、順滑模態控制、電動機研究趨勢與再生能源應用等最新研究與發展報告。研討會期間與研究領域相關的國外研究學者、專家相互討論能源轉換技術與再生能源新技術等相關問題，藉以提升在電力電子研究方面的深度與廣度。研討會中，針對筆者發表兩種不同方法的諧振式直流對直流轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此兩種電路架構都具有零電壓切換技術及高效率電路等優點，此兩種電路採用相同之控制方法在不同應用方面之優點有充分之說明與推論，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能。此次參加研討會獲得很多國外之研究成果，也詳細向國外學者介紹台灣之研究績效。

目次

一、 目的

參加二〇一四年IEEE-ICIT國際研討會之主要目的為1.發表研究實驗室近幾年來之研究成果，2.學習世界各專家學者與研究單位的研究方向與成果，3.與國際學者廣泛討論再生能源之科技趨勢，4.向各國專家學者說明與介紹台灣目前在高效率電源轉換器與再生能源技術研究之成果。

二、 過程

二〇一四年IEEE-ICIT國際研討會在韓國/釜山召開，會議時間自2月27日至3月2日。主辦單位為IEEE工業電子協會，協辦單位為IEEE韓國區分會，承辦單位為韓國高等科技學院。ICIT國際學術研討會是每年舉辦一次的國際學術研討會，每年會議在世界各國家舉辦(明年會議將在三月於西班牙Sevilla市舉辦)。此次研討會投稿篇數為三百多篇，投稿全文經三位審稿者無記名審查，通過審查共有一百七十多篇論文於會議中發表。會議中安排有五場主題演講，會議內容共有27個時段論文的口頭發表及3個時段海報張貼方式的論文發表。

2/27 日至 3/1 日參加各場次之論文發表會，筆者於研討會會中發表兩篇論文:

1. New Interleaved Three-Level ZVS Converter
2. New Series Half-Bridge Converters with the Balance Input Split Capacitor Voltages

筆者論文中發表兩種不同方法的高效率高壓直流轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此兩種電路架構都具有流電壓及零電流切換技術，此兩種電路採用不同之控制方法，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能，此兩篇文章獲得與會各國教授熱烈討論與互相交流，其中第二篇論文獲得大會之最佳論文獎。該會議為一有關之工業電子應用之 IEEE 國際研討會，會議內容包含電力電子，電力系統，IC 設計，影像處理，通信系統，控制工程等應用。

三、 心得

2014 年 IEEE-ICIT 為世界上有關工業電機電子相關研究方面重要會議之一。本次會議共有一百七十多篇論文，韓國是投稿篇數較多的國家，大陸與台灣在國際研討會的參與度相當積極，為提高台灣之學術地位及能見度，需國科會、教育部及各學術單位的補助以參加此等會議。在本次的會議中可以看出論文廣度加大，在會議中認識其他國家的人士，彼此交換心得，對於開拓視野、提升研究品質有莫大的幫助。此次會議之人員安排及會議過程順利，茲將出席本次會議心得分

述如下：

1．台灣學者在研究深度上與各國相比較，表現很好。

2.高效率電源器術在會議中討論踴躍，消費型電源技術有多篇在會議中發表，筆者在此方面之技術受到 IEEE-IE 及 PE 期刊副主編學者們肯定。

3. 會中與各國專家學者交換高效率電源轉換器與再生能源技術，獲益良多。

4. 與中國、日本及韓國學者在大會上廣泛互動與討論研究方向，作為將來合作之機會。

5. 此次會議中較多研究論文發表集中再生能源發電系統，利用高效能轉換器技術讓整體電源技術之效率提升，利用智慧型控制理論，增加實用性之產品應用。

6.傳統電力穩定度控制也是主要論文發表重點，利用智慧型控制方法，讓電力控制更有效力。

7.雲端電源技術之發展，在此次研討會中也是被討論主題之一。

8.大型高瓦數電動機控制系統在研討會中也受到相當之重視。

四、 建議事項

IEEE-ICIT 國際會議為 IEEE 有關電機電子相關研究方面重要的國際會議，所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對工業升級及發展高科技所需的高效率電源及驅動系統之發展，均有相當的影響。由於參與類似的學術性會議非常重要，故有以下建議:

1. 鼓勵學者積極參與國際學術會議。

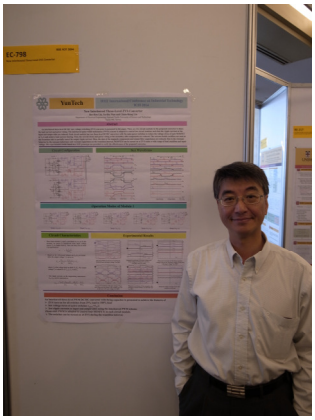
2. 政府應對此領域之研究多作投資。

3.中國學者出席國際研討會近幾年相當積極，人數超出台灣學者很多，台灣在此方面要多鼓勵國內學者出席介紹台灣教學研究成果。

五、 附錄

最佳論文獎獎狀及發表論文資料。

大會會場



論文發表現場

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Busan, Korea, February 26 - March 1, 2014

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2014 IEEE International Conference on Industrial Technology (ICIT), Feb. 26 - Mar. 1, 2014, Busan, Korea

New Interleaved Three-Level ZVS Converter

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***Abstract*—An interleaved three-level DC/DC zero voltage switching (ZVS) converter is presented in this paper. There are two circuit modules in the proposed converter to share the load current and power rating. The interleaved pulse-width modulation (PWM) scheme is adopted to control two circuit modules such that the ripple currents at the input and output sides are reduced. Each circuit module has two three-level DC/DC converters with the same power switches to reduce the voltage stress of each MOSFET at $V_{in}/2$ and achieve load current sharing. Thus, the current stress and power rating at the secondary side components are reduced. The current double rectifiers are used at the secondary side to partially cancel the output ripple current. Thus, the sizes of the magnetic components and output filter capacitance are reduced. Due to the resonant behavior by the resonant inductance and resonant capacitance at the transition interval, MOSFETs can be turned on at ZVS under a wide range of load condition and input voltage. The experimental results based on a 1*k*W prototype are provided to verify the effectiveness of the proposed converter.**

I. INTRODUCTION

Multilevel converters/inverters [1]-[3] have been proposed to reduce the voltage stress of power switches for high voltage and medium/high power applications. For modern switching mode power supplies such as the cloud server power unit and telecommunication applications, the high efficiency and high power density DC/DC converters have been demanded to meet the efficiency requirements of the Environment Protection Agency (EPA) and Climate Saver Computing Initiative (CSCI). Three-level DC/DC converters have been proposed in [4]-[5] to reduce the voltage stress of power switches at $V_{in}/2$. Thus, MOSFETs with voltage stress 600V can be used in the rear DC/DC converter. However, switches are operated in the hard switching such that the circuit efficiency is low if the high switching frequency is adopted. Three-level soft switching DC/DC converters [6]-[9] have been proposed to meet the demand of high circuit efficiency, small volume and light weight. Thus, all power switches can be turned on at zero current switching (ZCS) or zero voltage switching (ZVS) at the desired load range. The leakage inductance of the transformer (or external inductance) and the output capacitance of power switches are resonant at the transition interval such that the drain-to-source voltage of MOSFETs can be decreased to zero voltage before the MOSFETs are turned on. Thus, MOSFETs can be turned on at ZVS and the circuit efficiency is improved for high switching frequency. In the secondary side, the center-tapped rectifier can be used to regulate output voltage, smooth the output current and have one diode voltage drop. However, the drawback of the center-tapped rectifier is the high voltage stress on the rectifier diodes. The current doubler rectifier has one voltage drop, low output ripple current and low current stress of the output filter inductors. Thus, the current doubler rectifier has high efficiency compared with the center-tapper rectifier for high output current applications.

This paper presents an interleaved three-level DC/DC ZVS converter for high voltage and medium power applications. There are two circuit modules operated by an interleaved PWM scheme to share load current and reduce the ripple currents at the input and output capacitors. Thus, the size of the input and output capacitors can be reduced. For each circuit module, two three-level PWM circuits with current double rectifiers share the same power switches and reduce the current stress of the transformer windings, rectifier diodes and output filter inductors. The voltage stress of each MOSFET is clamped at one-half of the input voltage. Based on the resonant behavior by the output capacitance of MOSFETs and the leakage inductance of the transformer (or external inductance), all MOSFETs can be turned on at ZVS at the wide ranges of load current and input voltage. The operation principle, circuit analysis and design example of the proposed converter are discussed in detail. Finally, experiments with a 1*k*W prototype are provided to verify the effectiveness of the proposed converter.

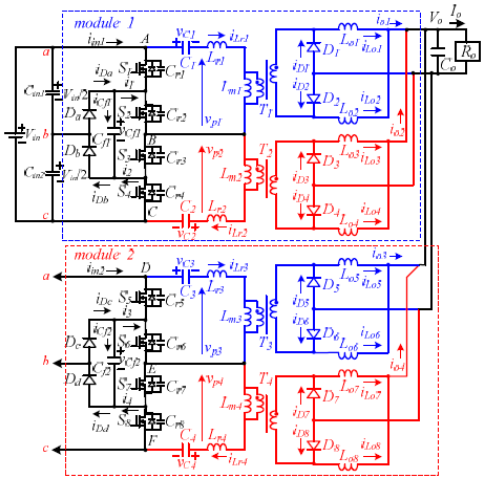

Fig. 1 The circuit configuration of the proposed interleaved three-level PWM DC/DC ZVS converter.

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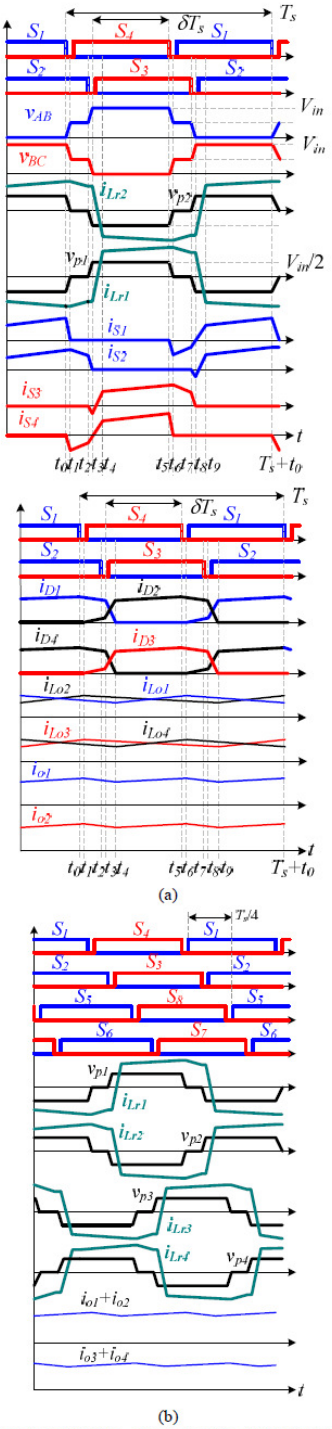


Fig. 2 PWM waveforms (a) the circuit module 1 (b) key waveforms of the proposed interleaved DC/DC converter.

I. CIRCUIT CONFIGURATION

Fig.1 gives the circuit configuration of the proposed ZVS converter. There are two circuit modules in the proposed converter to share load current for high input voltage and the medium/high power applications. The interleaved PWM with the phase-shift of 90 degrees is adopted to control two circuit modules. Thus, the ripple currents at the input and output capacitors are reduced. In each circuit module, there are two three-level PWM circuits with the same power switches to achieve ZVS turn-on for all switches, clamp the voltage stress of MOSFETs at $V_{in}/2$ and share the load current. In the first module, the components of the first three-level PWM circuit include C_{in1}, C_{in2}, D_a, D_b, C_{f1}, S_1-S_4, C_{r1}-C_{r4}, C_1, L_{r1}, T_1, D_1-D_2, L_{o1} and L_{o2}. The second three-level circuit includes the components of C_{in1}, C_{in2}, D_a, D_b, C_{f1}, S_1-S_4, C_{r1}-C_{r4}, C_2, L_{r2}, T_2, D_3-D_4, L_{o3} and L_{o4}. Three voltage levels V_{in}, $V_{in}/2$ and 0 are generated on the voltages v_{AB} and v_{BC}. Since the average voltages V_{C1}=V_{C2}=$V_{in}/2$, three voltage levels $V_{in}/2$, 0 and -$V_{in}/2$ are generated on the primary side voltages v_{p1} and v_{p2}. The current double rectifiers are adopted at the secondary side to obtain a stable output voltage V_o with one diode conduction loss and partially cancel the output ripple current. In the same manner, the second module includes the components of C_{in1}, C_{in2}, D_c, D_d, C_{f2}, S_5-S_8, C_{r5}-C_{r8}, C_3-C_4, L_{r3}-L_{r4}, T_3-T_4, D_5-D_8 and L_{o5}-L_{o8}. In the proposed converter, C_{in1} and C_{in2} are large enough to share the input voltage v_{Cin1}=v_{Cin2}=$V_{in}/2$. S_1-S_8 are power MOSFETs with the voltage stresses $V_{in}/2$. C_{r1}-C_{r8} are the output capacitances of MOSFETs S_1-S_8, respectively. D_a-D_d are the clamped diodes. C_{f1} and C_{f2} are the flying capacitances with the average voltages V_{Cf1}=V_{Cf2}=$V_{in}/2$. C_1-C_4 are the DC blocking capacitances with the average capacitor voltages V_{C1}=….=V_{C4}=$V_{in}/2$. L_{r1}-L_{r4} are the resonant inductances. L_{m1}-L_{m4} are the magnetizing inductances of the transformers T_1-T_4, respectively. D_1-D_8 are the rectifier diodes. L_{o1}-L_{o8} are the output filter inductances. R_o and C_o denote the load resistance and output capacitance.

II. OPERATION PRINCIPLE

Fig. 2(a) shows the theoretical PWM waveforms of the circuit module 1 in a switching period. Two circuit modules are operated with the interleaved PWM operation by the phase-shift of $T_s/4$ where T_s is a switching period. Fig. 2(b) gives the key waveforms of the proposed interleaved DC/DC converter. Some assumptions are made to discuss the system analysis.

(1) Power semiconductors S_1-S_8, D_1-D_8 and D_a-D_d are ideal.
(2) L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_m, L_{r1}=L_{r2}=L_{r3}=L_{r4}=L_r<<L_m and L_{o1}=….=L_{o8}=L_o.
(3) C_{in1}=C_{in2} are large enough to be considered as two voltage sources V_{Cin1}=V_{Cin2}=$V_{in}/2$ and C_{r1}=…..=C_{r8}=C_r.
(4) T_1 –T_4 have the same turns ratio n=n_p/n_s.
(5) C_1-C_4 and C_{f1}-C_{f2} are large enough to be treated as the constant voltages $V_{in}/2$.
(6) C_o is large enough to be considered as a constant output voltage V_o.

To simply the operation principle of the proposed converter, only circuit module 1 is discussed in the following. Based on

the on/off states of S_1-S_4, D_a-D_b and D_1-D_4, there are ten operation modes in circuit module 1 during a switching cycle. Fig. 3 shows the equivalent circuits of five operation modes in a half switching cycle. The operation of the second half switching cycle is symmetrical to the operation in the first half switching cycle. Thus, only five switching modes are discussed in the following. Prior to time t_0, S_1, S_2, D_1 and D_4 are conducting.

Mode 1 **[$t_0 \le t < t_1$]:** At time t_0, switch S_1 is turned off. Since $i_{Lr1}(t_0)<0$ and $i_{Lr2}(t_0)>0$, C_{r1} is charged linearly from zero voltage and C_{r4} is discharged linearly from $V_{in}/2$ via flying capacitor C_{fl}. The rising slope of the drain-to-source voltage of S_1 is limited by C_{r1} and C_{r4} such that switch S_1 is turned off at ZVS. If the energy stored in L_{r1}, L_{r2}, L_{o2} and L_{o3} are greater than the energy stored in C_{r1} and C_{r4}, then C_{r4} can be discharged to zero voltage. Thus, the ZVS turn-on condition of switch S_4 is expressed as:

$$(L_r + n^2 L_o)(i_{Lr1}^2(t_0) + i_{Lr2}^2(t_0)) \ge C_r V_{in}^2 / 2 \quad (1)$$

At time t_1, $v_{Cr1}=V_{in}/2$ and $v_{Cr4}=0$.

Mode 2 **[$t_1 \le t < t_2$]:** At t_1, $v_{Cr1}=V_{in}/2$, $v_{Cr4}=0$ and D_a is conducting. Since $i_{S4}(t_1)<0$, the anti-parallel diode of S_4 is conducting. Thus, S_4 can be turned on at this moment to achieve ZVS. In mode 2, $v_{AB}=v_{BC}=V_{in}/2$ and $v_{p1}=v_{p2}=0$. Thus, the primary and secondary winding voltages of T_1 and T_2 are all zero. D_1-D_4 are all conducting and $v_{Lo1}=v_{Lo2}=v_{Lo3}=v_{Lo4}=-V_o$ such that i_{Lo1}-i_{Lo4} decrease with the current slope of $-V_o/L_o$. Diode currents i_{D1} and i_{D4} decrease, and i_{D2} and i_{D3} increase in this time interval. The time interval in this mode is equal to $(0.5-\delta)T_s$ where δ is the duty ratio of the proposed converter when both S_1 and S_2 are in the on-state.

Mode 3 **[$t_2 \le t < t_3$]:** At t_2, S_2 is turned off. Since $i_{Lr1}(t_2)<0$ and $i_{Lr2}(t_2)>0$, C_{r2} and C_{r3} are charged and discharged, respectively. The rising slope of the drain-to-source voltage of S_2 is limited by C_{r2} and C_{r3} such that S_2 is turned off at ZVS. Since D_1-D_4 are still conducting, the primary and secondary windings of T_1 and T_2 are all zero voltage. If the energy stored in L_{r1} and L_{r2} are greater than the energy stored in C_{r2} and C_{r3}, then C_{r3} can be discharged to zero voltage. Therefore, the ZVS turn-on condition of S_3 is given as:

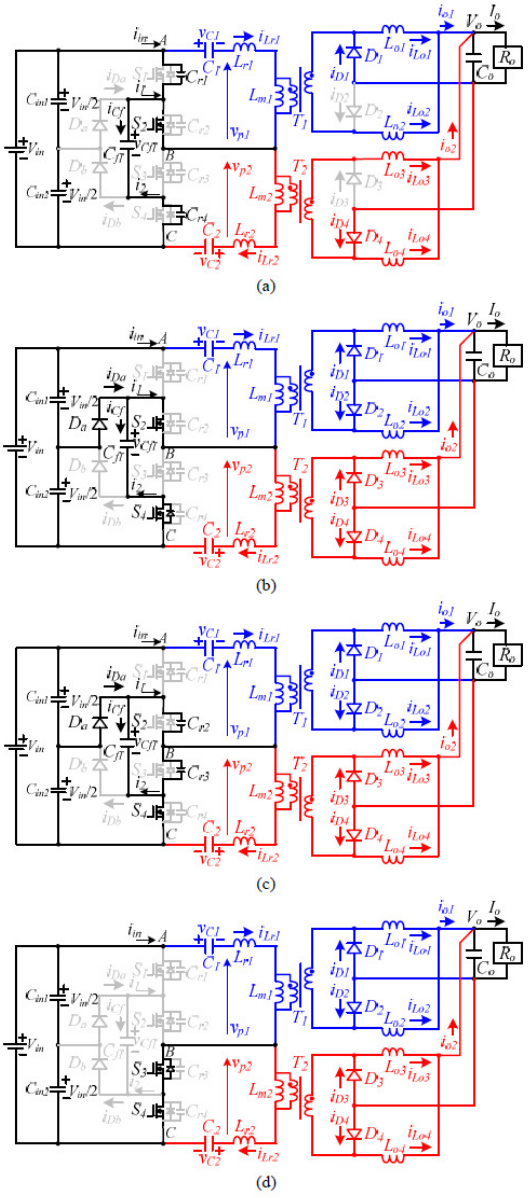
$$L_r(i_{Lr1}^2(t_2) + i_{Lr2}^2(t_2)) \ge C_r V_{in}^2 / 2 \quad (2)$$

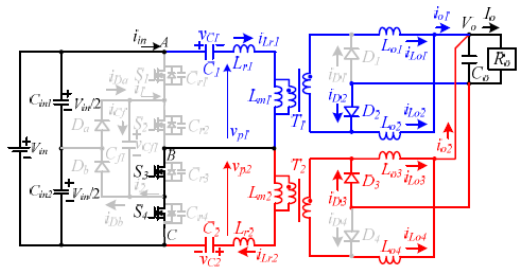
Mode 4 **[$t_3 \le t < t_4$]:** At t_3, $v_{Cr3}=0$. Since $i_{S3}(t_3)<0$, the anti-parallel diode of S_3 is conducting. Therefore, S_3 can be turned on at this moment to achieve ZVS. In this mode, the AC side voltages $v_{AB}=V_{in}$ and $v_{BC}=0$ such that the primary side voltages $v_{p1}=V_{in}/2$ and $v_{p2}=-V_{in}/2$. Since D_1-D_4 are still conducting in this mode, the primary and secondary winding voltages of T_1 and T_2 are all zero. Thus, $v_{Lr1}=V_{in}-V_{C1}=V_{in}/2$ and $v_{Lr2}=-V_{C2}=-V_{in}/2$. The inductor current i_{Lr1} increases linearly from $-i_{Lo2}/n$ to i_{Lo1}/n, and i_{Lr2} decreases linearly from i_{Lo3}/n to $-i_{Lo4}/n$ in this mode. Inductor currents i_{Lo1}-i_{Lo4} all decrease with the slope of $-V_o/L_o$. At time t_4, the diode currents i_{D1} and i_{D4} are decreased to zero. Since both switches S_3 and S_4 and diodes D_1-D_4 are in the on-state, no power is transferred from input voltage source V_{in} to output load R_o. Thus, the duty loss in mode 4 is expressed as:

$$\delta_{loss,4} \approx \frac{L_r I_o f_s}{2 n V_{in}} \quad (3)$$

where T_s and f_s are the switching period and switching frequency, respectively.

Mode 5 **[$t_4 \le t < t_5$]:** At t_4, $i_{D1}=i_{D4}=0$. T_1 and T_2 are working as the forward type transformers to transfer power from V_{in} to R_o. Thus, i_{Lr1} increases and i_{Lr2} decreases linearly. Power is transferred from V_{in} to R_o with the time interval $(\delta-\delta_{loss,4})T_s$. i_{Lo1} and i_{Lo4} increase, and i_{Lo2} and i_{Lo3} decrease in this mode.





(e)

Fig. 3 Operation modes of the circuit module 1 during first half switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5.

III. CIRCUIT CHARACTERISTICS

The circuit characteristics of the proposed converter are discussed in this section. Since the time intervals in modes 1, 3, 6 and 8 are much less than the turn-on time of three voltage levels on the transformer primary side, we neglect the effects of these four operation modes in the following discussion. Each circuit module provides one-half of load power. In modes 2 and 7 shown in Fig. 3, the average flying capacitor voltage can be obtained as V_{Cf1}=V_{Cf2}=V_{in}/2. From the volt-second balance on (L_{r1} and L_{m1}) and (L_{r2} and L_{m2}) in circuit module 1 and on (L_{r3} and L_{m3}) and (L_{r4} and L_{m4}) in circuit module 2, the average blocking capacitor voltages V_{C1}-V_{C4} are obtained as:

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{in}/2 \tag{4}$$

Based on the volt-second balance on L_{o1}-L_{o8} at steady state, the output voltage V_o is given as:

$$V_o = \frac{V_{in}}{2n}(\delta - \frac{L_r I_o f_s}{2nV_{in}}) - V_f \tag{5}$$

where V_f is the voltage drop on diode D_1-D_8. The output voltage V_o is related to δ, V_{in}, f_s, L_r, n and I_o. In steady state, the average output inductor currents I_{Lo1}=.....=I_{Lo8}=I_o/8. The ripple currents on L_{o1}-L_{o8} can be expressed as:

$$\Delta i_{Lo1} = ... = \Delta i_{Lo8} = \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{L_o V_{in}} \tag{6}$$

Thus, the output inductances L_{o1}=...=L_{o8}=L_o are given as:

$$L_o \geq \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{\Delta i_{Lo1,\max} V_{in}} \tag{7}$$

The ripple currents on the magnetizing inductances L_{m1}-L_{m4} can be expressed as:

$$\Delta i_{Lm} \approx \frac{V_{in}(\delta - \delta_{loss,4})T_s}{2L_m} = \frac{\delta V_{in} T_s}{2L_m} - \frac{L_r I_o}{4nL_m} \tag{8}$$

The average currents of D_1-D_8 are expressed as:

$$I_{D1,av} = ... = I_{D8,av} \approx I_o/8 \tag{9}$$

In modes 5 and 10, we can obtain the voltage stresses of D_1-D_8.

$$v_{D1,stress} = ... = v_{D8,stress} \approx V_{in}/2n \tag{10}$$

The peak currents of switches S_1-S_8 are approximately expressed as:

$$i_{S1,peak} = ... = i_{S8,peak}$$
$$\approx \frac{I_o}{4n} + \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{L_o V_{in}} + \frac{\delta V_{in} T_s}{2L_m} - \frac{L_r I_o}{4nL_m} \tag{11}$$

The root-mean-square (rms) currents of S_1-S_8 are approximately given as:

$$i_{S1,rms} = ... = i_{S8,rms} \approx \frac{I_o}{4n\sqrt{2}} \tag{12}$$

The voltage stresses of S_1-S_8 are clamped at V_{in}/2. At time t_0 (or t_0+T_s) in mode 10, the inductor currents $i_{Lr1}(t_0)$ and $i_{Lr2}(t_0)$ are expressed as:

$$i_{Lr1}(t_0) = i_{Lm1,\min} - \frac{i_{Lo2,\max}}{n}$$
$$= -\frac{\delta V_{in} T_s}{4L_m} + \frac{L_r I_o}{8nL_m} - \frac{I_o}{8n} - \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{2L_o V_{in}} \tag{13}$$

$$i_{Lr2}(t_0) = i_{Lm2,\max} + \frac{i_{Lo3,\max}}{n}$$
$$= \frac{\delta V_{in} T_s}{4L_m} - \frac{L_r I_o}{8nL_m} + \frac{I_o}{8n} + \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{2L_o V_{in}} \tag{14}$$

In the same manner, the inductor currents $i_{Lr1}(t_2)$ and $i_{Lr2}(t_2)$ in mode 2 are given as:

$$i_{Lr1}(t_2) \approx -\frac{\delta V_{in} T_s}{4L_m} + \frac{L_r I_o}{8nL_m} - \frac{I_o}{8n}$$
$$- \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{2L_o V_{in}} + \frac{(V_o + V_f)(0.5 - \delta)T_s}{nL_o} \tag{15}$$

$$i_{Lr2}(t_2) \approx \frac{\delta V_{in} T_s}{4L_m} - \frac{L_r I_o}{8nL_m} + \frac{I_o}{8n}$$
$$+ \frac{(V_o + V_f)T_s[V_{in} - 2n(V_o + V_f)]}{2L_o V_{in}} - \frac{(V_o + V_f)(0.5 - \delta)T_s}{nL_o} \tag{16}$$

With the derived inductor currents in (13)-(16), the necessary resonant inductance L_r can be obtained from (1) to achieve ZVS turn-on of S_1, S_4, S_5 and S_8 and from (2) to achieve ZVS turn-on of S_2, S_3, S_6 and S_7.

IV. EXPERIMENTAL RESULTS

In this section, the experimental results based on a prototype circuit are provided to verify the effectiveness of the proposed converter. The specifications of the prototype circuit are V_{in}=480V-580V, V_o=24V, P_o=1kW and f_s=100kHz. Therefore, the power rating of each circuit module is 500W. Fig. 4 gives the measured PWM waveforms of switches S_1-S_8 at full load and high input voltages. The PWM signals of S_5-S_8 are phase-shifted one-fourth of switching period with respective to the PWM signals of S_1-S_4. Figs. 5 and 6 give the measured results of the gate voltage and drain voltage of switches S_1 and S_2 at 25% load with low and high input voltages, respectively. It is clear in Figs. 5 and 6 that the switches S_1 and S_2 are all turned on at ZVS from 25% load to 100% load. The voltage stress of both switches S_1 and S_2 is V_{in}/2. Since the PWM waveforms of S_3 and S_4 and the PWM waveforms of S_2 and S_1 are identical, it is clear that S_3 and S_4 can achieve ZVS from 25% to 100% loads. Fig. 7 gives the

measured waveforms of the flying capacitor voltages and the DC blocking voltages at full load with high input voltage. All of these voltages are equal to $V_{in}/2$. Fig. 8 illustrates the measured results of the gate voltages $v_{S1,gs}$ and $v_{S2,gs}$ and the primary side voltages v_{p1}-v_{p4} at full load and V_{in}=580V. There are three voltage levels on the primary side voltages v_{p1}-v_{p4}. The measured waveforms of the primary side currents at full load and V_{in}=580V are shown in Fig. 9. The current waveforms in the primary side of two circuit modules are balanced and phase-shifted by one-fourth of switching period. Fig. 10 shows the measured results of the secondary side currents of circuit module 1 at full load and V_{in}=580V. The output diode currents and the filter inductor currents of two current doubler rectifiers are balanced. Fig. 11 illustrates the measured output currents of two circuit modules at full load and V_{in}=580V. It is clear that the output currents of two circuit modules are balanced.

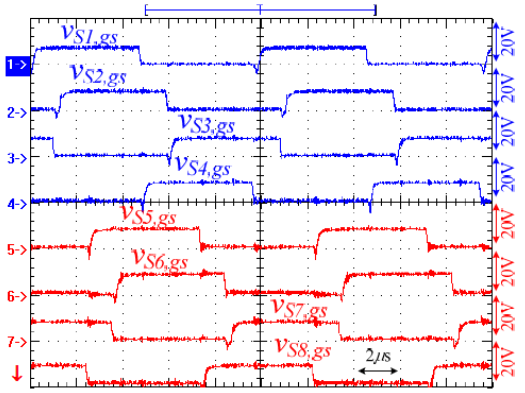


Fig. 4 Measured PWM waveforms of switches S_1-S_8 at full load with input voltage V_{in}=580V.

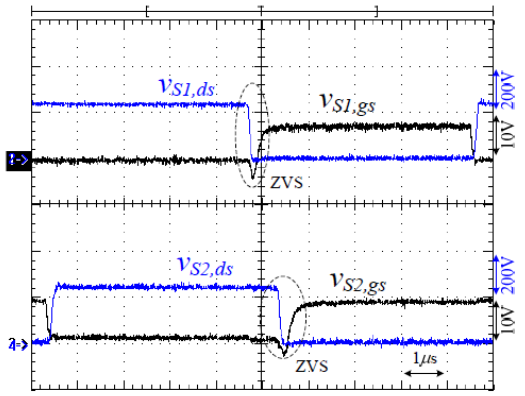


Fig. 5 Measured waveforms of the gate voltage and drain voltage of switches S_1 and S_2 at V_{in}=480V and 25% load.

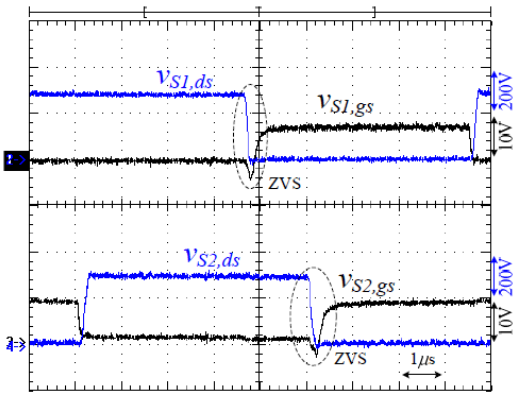


Fig. 6 Measured waveforms of the gate voltage and drain voltage of switches S_1 and S_2 at V_{in}=580V and 25% load.

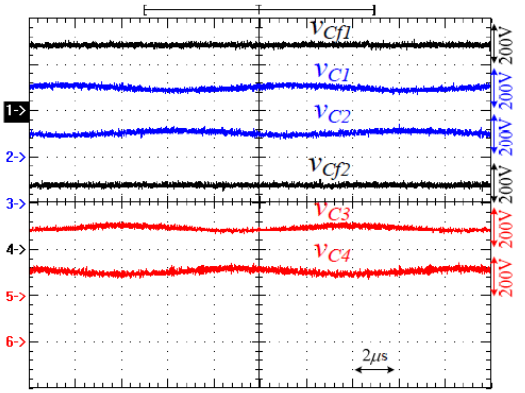


Fig. 7 Measured waveforms of the flying capacitor voltages and the DC blocking voltages at full load with input voltage V_{in}=580V.

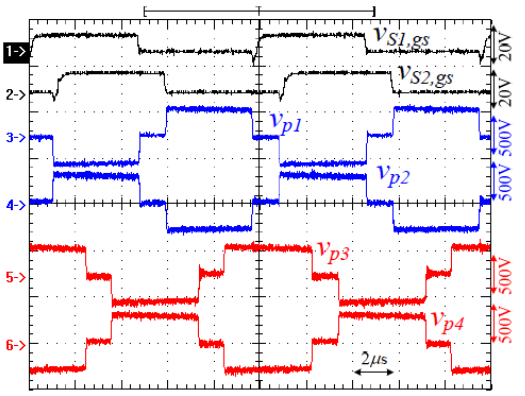


Fig. 8 Measured waveforms of the gate voltages $v_{S1,gs}$ and $v_{S2,gs}$ and the primary side voltages v_{p1}-v_{p4} at full load with input voltage V_{in}=580V.

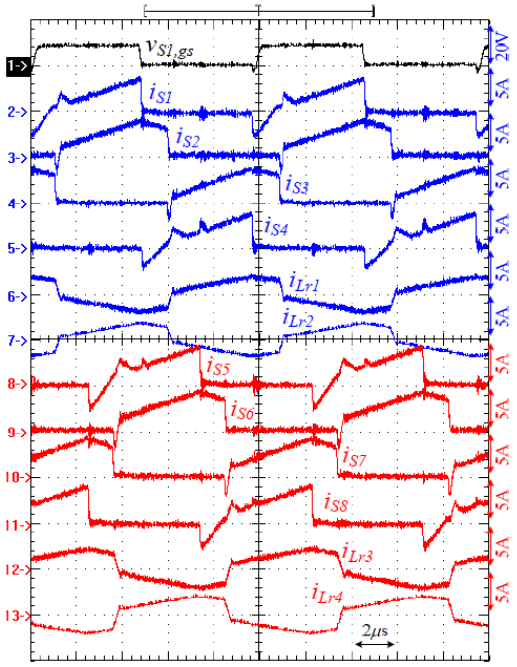


Fig. 9 Measured waveforms of the primary side currents at 100% load.

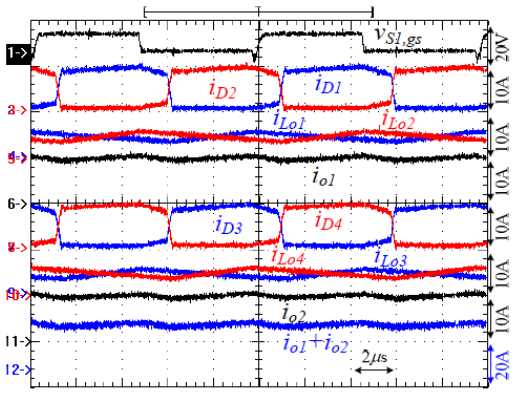


Fig. 10 Measured waveforms of the secondary side currents of circuit module 1 at full load and V_{in}=580V.

V. CONCLUSION

An interleaved three-level PWM DC/DC converter with flying capacitor is presented to achieve the features of 1) ZVS turn-on for all switches from 25% load to 100% load, 2) low voltage stress of active switches $v_{stress}=V_{in}/2$, and 3) low ripple currents at input and output sides using the interleaved PWM scheme. Phase-shift PWM is adopted to control four MOSFETs in each circuit module. Thus the switches can be turned on at ZVS during the transition interval. The system analysis, operation mode, circuit characteristics and design example of the proposed converter are discussed in detail. Finally, experiments with 1*k*W prototype are provided to verify the effectiveness of the proposed converter.

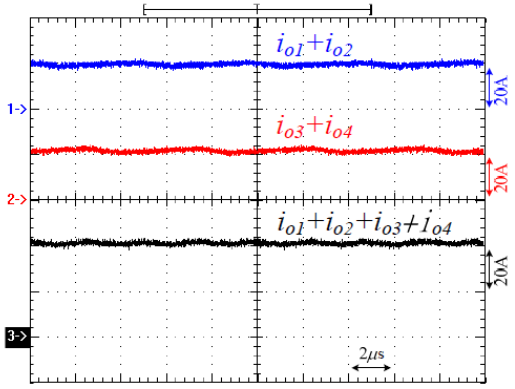


Fig. 11 Measured output currents of two circuit modules at full load.

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New Series Half-Bridge Converters with the Balance Input Split Capacitor Voltages

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***Abstract*—A new DC/DC converter is presented for high input voltage and high load current applications. In order to reduce the converter size and achieve high circuit efficiency, MOSFETs with high switching frequency are adopted in the converter. To achieve high circuit efficiency, two half-bridge converters are connected in series to reduce the voltage rating of power switches and asymmetric pulse-width modulation is adopted to control output voltage and achieve zero voltage switching turn-on for all power switches. In order to share the load current and reduce the current rating of rectifier diodes for high output current applications, two center-tapped rectifiers are connected in parallel. The series-connected transformers at high voltage side are used to balance two output inductor currents. Two series capacitors are connected at the AC terminals of two half-bridge converters to balance two input capacitor voltages in every switching cycle. The output capacitances of MOSFETs and the resonant inductances are resonant at the transition instant such that MOSFETs can be turned on at zero voltage switching. Finally, experiments based on a laboratory prototype with 1*k*W rated power are provided to verify the effectiveness of proposed converter.**

***Keywords*—DC-DC Converter, ZVS.**

I. INTRODUCTION

Recently high input DC converters have been studied and developed for many industry applications such as ship electric power distribution system [1], three-phase switching mode power supplies, and high speed railway electrical system [2]. Thus, power switches with high voltage rating and low switching frequency are used for high input voltage applications. Three-level converters/inverters [3]-[7] based on neutral-point diode clamp, capacitor clamp or series H-bridge topologies have been developed to reduce and limit the voltage rating of power devices. For modern power converters, the compact size, high power density and high circuit efficiency are normally demanded. In order to achieve high power density and compact size for high voltage applications, power switches with high switching frequency and low voltage rating such as MOSFETs are adopted in three-level converters. By using the more MOSFETs, split capacitors and clamp diodes, the voltage stress of each MOSFET can be reduced to one-half of DC bus voltage. Therefore MOSFETs with 600V voltage stress can be used in the rear DC/DC converter for high input voltage applications. The phase-shift PWM IC was normally adopted to generate four PWM signals for power switches with ZVS turn-on at the designed load range. The center-tapped rectifier or diode bridge rectifier is adopted in the secondary side for low voltage or high voltage application. Compared to the two-level converters, the three-level converters have more circuit components and high cost. Three-level zero voltage switching (ZVS) converters [8]-[13] have been developed to reduce the switching losses on power switches such that power converter with high circuit efficiency can be achieved.

A new soft switching DC converter is presented in this paper for high input voltage and high load current applications. The main advantages of the proposed converter are low switching losses, ZVS turn-on and low voltage rating of MOSFETs. Two input capacitors and two half-bridge converters are connected in series at high voltage side to reduce the voltage rating of MOSFETs at $V_{in}/2$. Thus, power MOSFETs with 500V voltage rating can be used in DC converters with 1000V input voltage. In order to balance two input capacitor voltages, two balance capacitors are connected in series between the AC sides of two half-bridge legs. Therefore, two input capacitor voltages can be automatically balanced in each switching cycle. Two center-tapper rectifiers are adopted to reduce the current rating of the transformer windings and rectifier diodes. The primary windings of two transformers are connected in series in order to balance the secondary winding currents. Thus, power can be equally transferred to output load through two center-tapped rectifiers. Asymmetric pulse-width modulation is adopted to control four MOSFETs. MOSFETs can be turned on under ZVS at the transition interval due to the resonant behavior by output capacitance of MOSFETs and resonant inductance. Experiments with a laboratory prototype are presented to demonstrate the performance of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig. 1(a) gives the circuit configuration of the conventional half-bridge converter with APWM scheme to achieve ZVS turn-on for all switches. The voltage stress of power switches is equal to V_{in}. Power MOSFETs with 600V voltage stress are normally adopted in the APWM half-bridge converter which is used after the single-phase power factor corrector. If the three-phase AC/DC converter with power factor correction is necessary in the switching mode power supplies, then the 900V voltage stress MOSFETs or 1200V IGBTs should be used in the second stage DC/DC converter. In order to use the low voltage stress MOSFETs and high switching frequency, two APWM half-bridge converters shown in Fig. 1(b) are connected in series at high voltage side to reduce the voltage rating of power switches and connected in parallel at low voltage side to reduce the current rating of passive and active components. Thus, the voltage stress of each power switch is

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equal to $V_{in}/2$. However, the input two split capacitor voltages can be unbalanced and will result in the unbalanced output inductor currents.

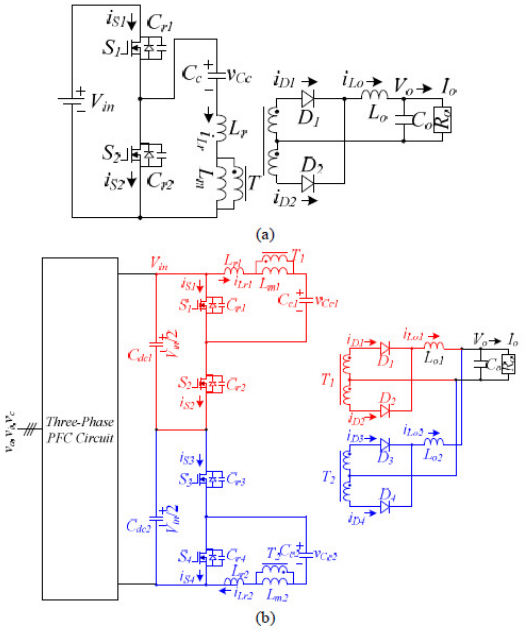


Fig. 1 Circuit configuration (a) asymmetric half-bridge converter (b) two series asymmetric half-bridge converters.

Fig. 2 shows the circuit configuration of the proposed converter. The DC bus voltage after the three-phase power factor corrector is normally in the range of 750V-800V. Two input split capacitor voltages V_{Cdc1} and V_{Cdc2} can be automatically balanced by two DC clamped capacitors C_{c1} and C_{c2}. There are two series half-bridge converters in the proposed converter. The first half-bridge converter includes C_{dc1}, S_1, S_2, L_r, T_1, T_2, C_{r1}, C_{r2}, C_{c1}, D_1, D_2, L_{o1} and C_o. The second half-bridge converter includes the components of C_{dc2}, S_3, S_4, L_r, T_1, T_2, C_{r3}, C_{r4}, C_{c2}, D_3, D_4, L_{o2} and C_o. V_{in} is the input DC bus voltage and V_o is the output voltage. C_o is output capacitance and R_o is load resistance. C_{c1} and C_{c2} are DC blocking capacitances. C_{r1}-C_{r4} are output capacitances of MOSFETs S_1-S_4, respectively. L_r is resonant inductance. L_{m1} and L_{m2} are the magnetizing inductances of transformers T_1 and T_2, respectively. L_{o1} and L_{o2} are output inductances. D_1-D_4 are rectifier diodes. Asymmetric PWM scheme is used to control MOSFETs S_1-S_4. S_1 and S_3 have the same PWM signals and S_2 and S_4 have the same PWM waveforms. However, S_1 and S_2 are complementary each other with a dead time to allow ZVS operation. C_{dc1} and C_{dc2} are input capacitors to split the input voltage (V_{Cdc1}=V_{Cdc2}=V_{in}/2). C_{c1} and C_{c2} are connected in series between the AC terminals a and b in order to automatically balance two input split capacitor voltages V_{Cdc1} and V_{Cdc2}. If S_1 and S_3 are conducting and S_2 and S_4 are in the off-state, then the voltage across C_{c1} and C_{c2} is equal to V_{Cdc1} and the voltage stresses of S_2 and S_4 are equal to V_{Cdc1} and V_{Cdc2}, respectively. If S_1 and S_3 are in the off-state and S_2 and S_4 are in the off-state, then the voltage across C_{c1} and C_{c2} is equal to V_{Cdc2} and the voltage stresses of S_1 and S_3 are equal to V_{Cdc1} and V_{Cdc2}, respectively. Based on the on/off states of S_1-S_4, two split capacitor voltages V_{Cdc1}=V_{Cdc2}=V_{in}/2 and the voltage stress of S_1-S_4 is equal to V_{in}/2.

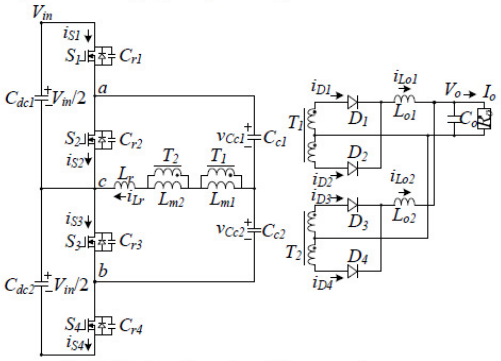


Fig. 2 Circuit configuration of the proposed converter.

III. Operation Principle

Fig. 3 shows the key waveforms of the proposed converter in a switching cycle. The duty cycle of S_1 and S_3 is δ, and the duty cycle of S_2 and S_4 is 1-δ. Before the discussion of the proposed converter, the following assumptions are made to simplify the system analysis. (a) Two isolated transformers T_1 and T_2 are identical with the magnetizing inductances L_{m1}=L_{m2}=L_m and the turns ratio n=n_p/n_{s1}=n_p/n_{s2}, (b) power switches S_1-S_4 and rectifier diodes D_1-D_4 are ideal, (c) resonant capacitances C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r, (d) DC blocking capacitances C_{c1}=C_{c2}=C_c, (e) input split capacitances C_{dc1}=C_{dc2}, (f) output inductances L_{o1}=L_{o2}, and (g) the energy stored in resonant inductances is greater than the energy stored in resonant capacitances such that the ZVS turn-on of all switches can be achieved. Based on the on/off states of S_1-S_4 and D_1-D_4, the proposed converter has eight operating modes during one switching cycle. Fig. 4 illustrates the corresponding equivalent circuits of eight operation modes. Before time t_0, S_1, S_3 and D_1-D_4 are conducting.

Mode 1 [t_0≤t<t_1, Fig. 4(a)]: At t_0, i_{D2}=i_{D4}=0 such that D_2 and D_4 are turned off. Since L_{m1}=L_{m2}>>L_r, v_{Lm1}=v_{Lm2}=v_{Cc2}/2=(V_{in}/2-v_{Cc1})/2. The output inductor currents i_{Lo1} and i_{Lo2} both increase with the slope of [(V_{in}/2-v_{Cc1})/2n-V_o]/L_o. Power is transferred from C_{dc1} and C_{c2} to R_o through S_1, S_3, C_{c1}, C_{c2}, T_1, T_2, L_r, D_1, D_3, L_{o1} and L_{o2}. This mode ends at t_1 when S_1 and S_3 are off.

Mode 2 [t_1≤t<t_2, Fig. 4(b)]: At t_1, S_1 and S_3 are off. Since i_{Lr}(t_1)>0, C_{r1} and C_{r3} are charged linearly, and C_{r2} and C_{r4} are discharged linearly. This mode ends at t_2 when v_{Cr2}=v_{Cc1} and v_{Cr3}=v_{Cc2}.

Mode 3 [t_2≤t<t_3, Fig. 4(c)]: At t_2, v_{Cr2}=v_{Cc1} and v_{Cr3}=v_{Cc2}. Thus, the primary and secondary winding voltages of T_1 and T_2 are equal to zero voltage and diodes D_1-D_4 are all conducting. The output inductor voltages v_{Lo1} and v_{Lo2} are equal to -V_o and the inductor currents i_{Lo1} and i_{Lo2} both decrease. Diode currents i_{D1}

and i_{D3} decrease, and i_{D2} and i_{D4} increase in this mode. C_{r1} and C_{r3} are continuously charged, and C_{r2} and C_{r4} are discharged in this mode. If the energy stored in L_r is greater than the energy stored in C_{r1}-C_{r4}, then C_{r2} and C_{r4} can be discharged to zero voltage. At t_3, v_{Cr2}=v_{Cr4}=0. The time interval in modes 2 and 3 can be expressed as:

$$\Delta t_{13} = t_3 - t_1 \approx \frac{2C_r V_{in}}{i_{Lr}(t_1)} \tag{1}$$

In order to turn on S_2 and S_4 under ZVS, the dead time t_d between S_1 and S_2 should be greater than the time interval Δt_{13}.

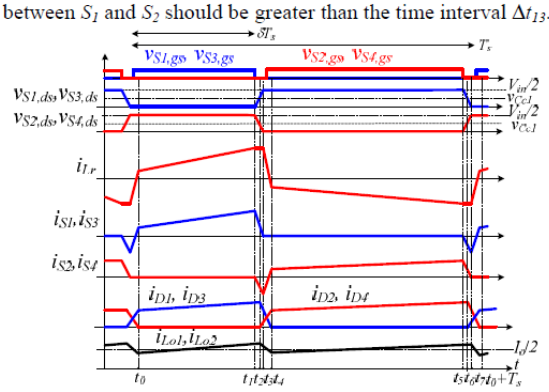
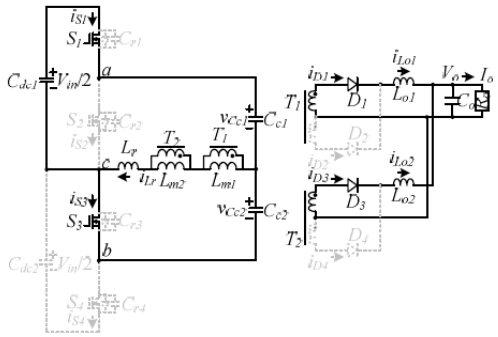
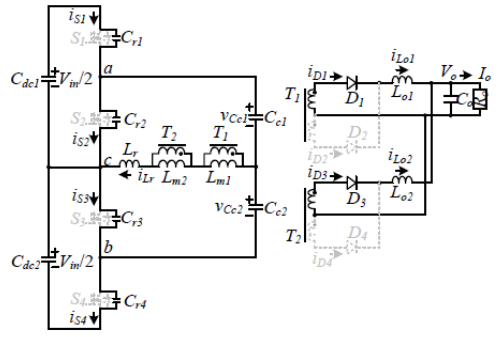
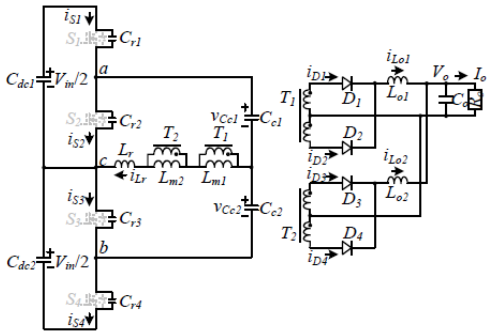
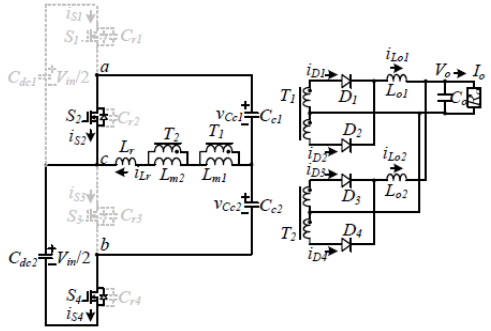


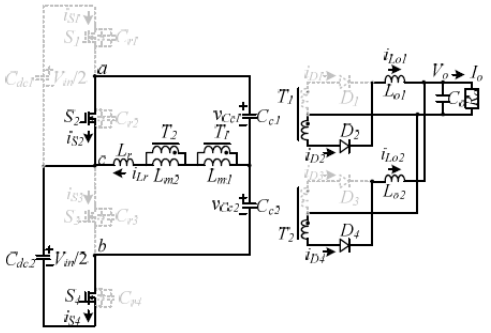
Fig. 3 Key waveforms of the proposed converter.

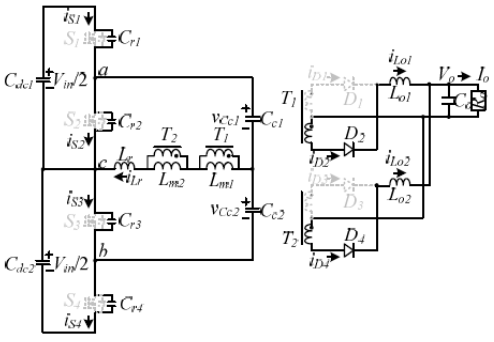


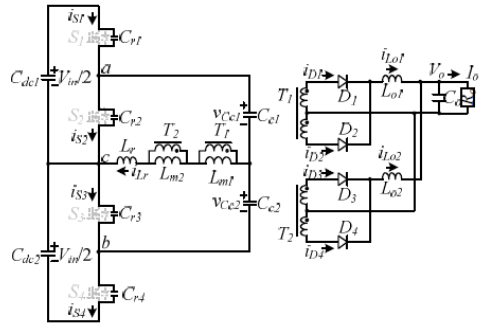




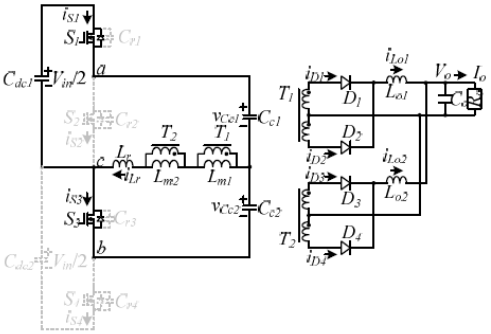








(g)



(h)

Fig. 4 Operation modes of the proposed converter in a switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8.

Mode 4 [$t_3 \le t < t_4$, Fig. 4(d)]: At t_3, C_{r2} and C_{r4} are discharged to zero voltage. Since $i_{Lr}(t_3)$ is positive, the anti-parallel diodes of S_2 and S_4 are conducting at t_3. Thus, S_2 and S_4 can be turned on at this moment to achieve ZVS. Since D_1-D_4 are still in the commutation state, the inductor voltage $v_{Lr}=-(V_{in}/2-v_{Cc2})=-v_{Cc1}$. Thus, i_{Lr} decreases in this mode. At t_4, diode currents $i_{D1}=i_{D3}=0$. In this mode, the current variation on L_r is $\Delta i_{Lr} = I_o / n$. The time interval in this mode is given as:

$$\Delta t_{34} = t_4 - t_3 \approx \frac{L_r I_o}{n(V_{in}/2 - v_{Cc2})} = \frac{L_r I_o}{n v_{Cc1}} \tag{2}$$

In this mode, S_2 and S_4 are in the on-state and $v_{Lo1}=v_{Lo2}=-V_o$. Thus, the duty loss in mode 4 is given as:

$$\delta_{loss,4} = \frac{\Delta t_{34}}{T_s} \approx \frac{L_r I_o f_s}{n v_{Cc1}} \tag{3}$$

Mode 5 [$t_4 \le t < t_5$, Fig. 4(e)]: At t_4, i_{D1} and i_{D3} are decreasing to zero current. Thus, the inductor current i_{Lr} decreases in this mode. Since the duty ratio of S_1 and S_3 is less than 0.5, the average voltages of C_{c1} and C_{c2} are less and larger than $V_{in}/4$, respectively. Thus, the output inductor currents i_{Lo1} and i_{Lo2} decrease with the slope of $[v_{Cc1}/2n-V_o]/L_o$. Power is transferred from C_{dc2} and C_{c1} to R_o through S_2, S_4, C_{c1}, C_{c2}, T_1, T_2, L_r, D_2, D_4, L_{o1} and L_{o2}. At t_5, S_2 and S_4 are turned off.

Mode 6 [$t_5 \le t < t_6$, Fig. 4(f)]: At t_5, S_2 and S_4 are turned off. Since $i_{Lr}(t_5)<0$, C_{r2} and C_{r4} are charged, and C_{r1} and C_{r3} are discharged in this mode. In this mode, i_{Lr} is almost constant. At t_6, the capacitor voltages $v_{Cr2}=v_{Cc1}$ and $v_{Cr3}=v_{Cc2}$.

Mode 7 [$t_6 \le t < t_7$, Fig. 4(g)]: At t_6, $v_{Cr2}=v_{Cc1}$ and $v_{Cr3}=v_{Cc2}$. Therefore, the primary and secondary winding voltages of T_1 and T_2 are all equal to zero voltage. Diodes D_1-D_4 are conducting. The output inductor voltages $v_{Lo1}=v_{Lo2}=-V_o$ such that i_{Lo1} and i_{Lo2} both decrease. In this mode, i_{D1} and i_{D3} increase and i_{D2} and i_{D4} decrease. C_{r1} and C_{r3} are continuously discharged, and C_{r2} and C_{r4} are charged. C_{r1} and C_{r3} can be discharged to zero voltage if the energy stored in L_r is greater than the energy stored in C_{r1}-C_{r4}. At t_7, $v_{Cr1}=v_{Cr3}=0$. The time interval in modes 6 and 7 can be given as:

$$\Delta t_{57} = t_7 - t_5 \approx \frac{2 C_r V_{in}}{i_{Lr}(t_5)} \tag{4}$$

The dead time t_d between S_1 and S_2 should be greater than the time interval Δt_{57} in order to turn on S_1 and S_3 under ZVS.

Mode 8 [$t_7 \le t < t_0+T_s$, Fig. 4(h)]: At t_7, $v_{Cr1}=v_{Cr3}=0$. Since $i_{Lr}(t_7)$ is negative, the anti-parallel diodes of S_1 and S_3 are conducting. Therefore, S_1 and S_3 can be turned on at this moment under ZVS. Since D_1-D_4 are in the commutation state, the inductor voltage $v_{Lr}=(V_{in}/2-v_{Cc1})=v_{Cc2}$ and i_{Lr} increases in this mode. At t_0+T_s, diode currents $i_{D2}=i_{D4}=0$. The current variation on L_r is $\Delta i_{Lr} = I_o / n$ and the time interval in this mode is expressed as:

$$\Delta t_{70} = t_7 - t_0 \approx \frac{L_r I_o}{n(V_{in}/2 - v_{Cc1})} = \frac{L_r I_o}{n v_{Cc2}} \tag{5}$$

In this mode, S_1 and S_3 are in the on-state and $v_{Lo1}=v_{Lo2}=-V_o$. No power is transferred from input voltage V_{in} to output load R_o. Thus, the duty loss in mode 8 is given as:

$$\delta_{loss,8} = \frac{\Delta t_{70}}{T_s} \approx \frac{L_r I_o f_s}{n v_{Cc2}} \tag{6}$$

Then the circuit operations of the proposed converter in one switching cycle are completed.

IV. Circuit Characteristics

Since the capacitance of C_{r1}-C_{r4} are much less than the DC clamped capacitances C_{c1} and C_{c2}, the charged and discharged times of C_{r1}-C_{r4} at turn-on and turn-off instant in modes 2, 3, 6 and 7 can be neglected to derive the DC voltage conversion ratio. Thus, only modes 1, 4, 5 and 8 are considered in the following discussion. The key waveforms of the proposed converter under the simplified operation modes are shown in Fig. 5. From the volt-second balance on L_r, L_{m1} and L_{m2}, the average capacitor voltages V_{Cc1} and V_{Cc2} are derived as:

$$V_{Cc1} = \frac{\delta V_{in}}{2},\ V_{Cc2} = \frac{(1-\delta) V_{in}}{2} \tag{7}$$

where δ is the duty cycle of S_1 and S_3. Based on the volt-second balance on L_{o1} and L_{o2} at steady state, the DC voltage conversion ratio of the proposed converter can be derived as:

$$\frac{V_o + V_f}{V_{in}} = \frac{-2\delta^2 + \delta(2 + \delta_{loss,8} - \delta_{loss,4}) - \delta_{loss,8}}{4n} \tag{8}$$

where V_f is the voltage drop on each diode of D_1-D_4. The final output voltage V_o can be obtained from (3) and (6)-(8).

$$V_o = \frac{V_{in}}{2n}[\delta(1-\delta) - \frac{2L_r I_o f_s}{nV_{in}}] - V_f \quad (9)$$

From (9), the output voltage V_o is a function of duty cycle δ, input voltage V_{in}, switching frequency f_s, resonant inductance L_r, turns ratio n and load current I_o. The average output inductor currents under the steady state are $I_{Lo1}=I_{Lo2}=I_o/2$. The ripple currents of output inductors are give as:

$$\Delta i_{Lo1} = \Delta i_{Lo2} \approx \frac{(V_{in}/2 - V_{Cc1})/(2n) - (V_o + V_f)}{L_o}(\delta - \delta_{loss,\delta})T_s \quad (10)$$
$$= \frac{V_{in}T_s}{4nL_o}[\delta(1-\delta)(1-2\delta) + \frac{2L_r I_o f_s(3\delta-1)}{nV_{in}} - \frac{4}{1-\delta}(\frac{L_r I_o f_s}{nV_{in}})^2]$$

Due to $i_{Cc1,av}=i_{Cc2,av}=0$, the average magnetizing current can be derived as $I_{Lm}\approx(1\text{-}2\delta)I_o/n$. The average diode currents are expressed as $i_{D1,av} = i_{D3,av} \approx \delta I_o/2$ and $i_{D2,av} = i_{D4,av} \approx (1-\delta)I_o/2$. The voltage stresses of rectifier diodes are obtained as $v_{D1,stress} = v_{D3,stress} \approx \delta V_{in}/n$ and $v_{D2,stress} = v_{D4,stress} \approx (1-\delta)V_{in}/n$. The *rms* currents of S_1-S_4 are expressed as $i_{S1,rms} = i_{S3,rms} \approx (3-4\delta)I_o\sqrt{\delta}/(2n)$ and $i_{S2,rms} = i_{S4,rms} \approx (4\delta-1)I_o\sqrt{1-\delta}/(2n)$. The voltage ratings of S_1-S_4 are clamped at $V_{in}/2$.

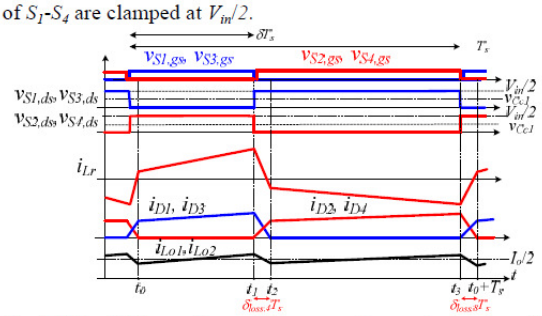


Fig. 5 Main PWM waveforms of the proposed converter based on the simplified operation modes.

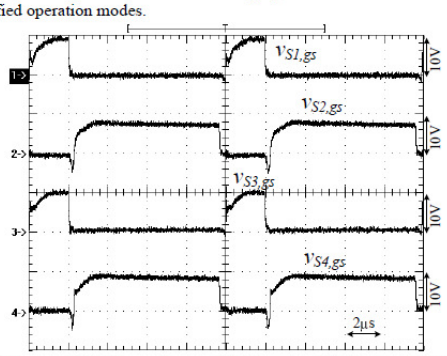


Fig. 6 Measured PWM waveforms of S_1-S_4 under 25% load and 800V input voltage

V. Experimental Results

Experiments based on a laboratory prototype are presented in this section to verify the effectiveness of the proposed converter for high input voltage applications. The circuit electric specifications are V_{in}=750-800V, V_o=24V, P_o=1*k*W. The switching frequency is 100*k*Hz. Power MOSFETs IRFP460 are used for active switches S_1-S_4. The DC blocking capacitances $C_{c1}=C_{c2}=200n$F. Input capacitances $C_{dc1}=C_{dc2}=680\mu$F. The resonant inductance $L_r=21\mu$H. Turns ratio of transformers of T_1 and T_2 is 22:10:10. The magnetizing inductances of T_1 and T_2 are $L_{m1}=L_{m2}=400\mu$H. The fast recovery diodes 60CPQ150 are used for D_1-D_4. The output inductances $L_{o1}=L_{o2}$ =20μH. The output capacitance is C_o=4400μF. Fig. 6 illustrates the measured PWM waveforms of S_1-S_4 at 25% load. Fig. 7 gives the measured gate voltage, drain voltage and switch current of switches S_1-S_4 at V_{in}=800V and 25% load condition. The drain voltages $v_{S1,ds}$-$v_{S4,ds}$ have been decreased to zero voltage before switches S_1-S_4 are turned on. Since power switches are difficult to achieve ZVS at light load and easy to implement ZVS at full load, it is clear that S_1-S_4 can be turned on under ZVS from 25% load from Fig. 7. Fig. 8 gives the measured voltage waveforms v_{Cdc1}, v_{Cdc2}, v_{Cc1}, v_{Cc2} and $v_{Cc1}+v_{Cc2}$ at full load. It can be observed that three voltages v_{Cdc1}, v_{Cdc2} and $v_{Cc1}+v_{Cc2}$ are balanced. Fig. 9 shows the measured waveforms of $v_{S1,gs}$, i_{Lr}, v_{Cc1} and v_{Cc2} at full load. When S_1 is in the on-state, i_{Lr} increases. On the other hand, i_{Lr} decreases if S_1 is in the off-state. Fig. 10 gives the measured waveforms of $v_{S1,gs}$, i_{D1}-i_{D4}, i_{Lo1} and i_{Lo2} at full load condition. Two output inductor currents i_{Lo1} and i_{Lo2} are balanced each other.

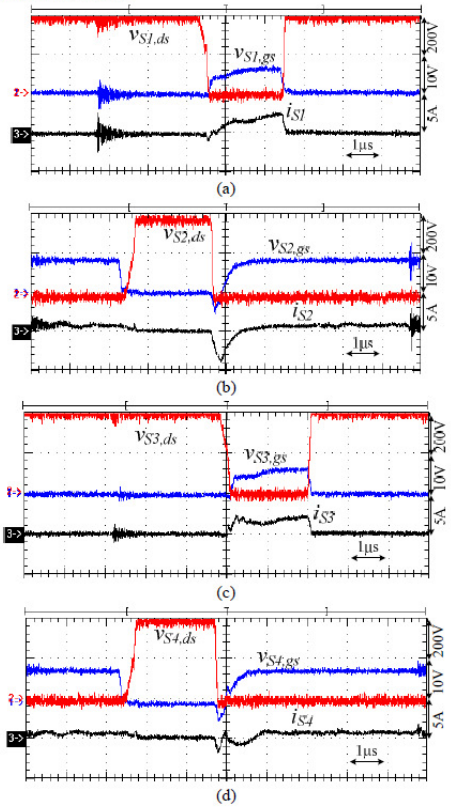


Fig. 7 Measured gate voltage, drain voltage and switch current of switches at V_{in}=800V and 25% load condition (a) S_1 (b) S_2 (c) S_3 (d) S_4.

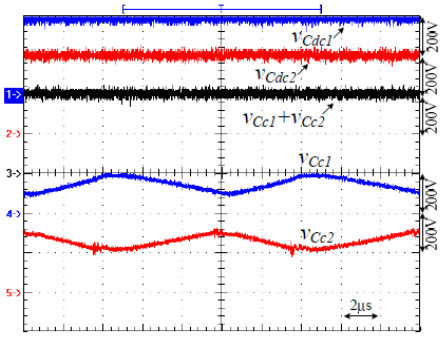


Fig. 8 Measured voltage waveforms v_{Cdc1}, v_{Cdc2}, v_{Cc1}, v_{Cc2} and $v_{Cc1}+v_{Cc2}$ at full load under 800V input voltage.

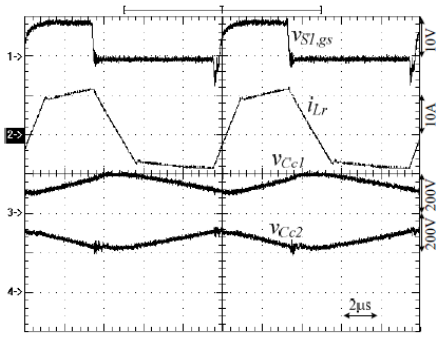


Fig. 9 Measured waveforms of $v_{S1,gs}$, i_{Lr}, v_{Cc1} and v_{Cc2} at 800V input voltage and full load.

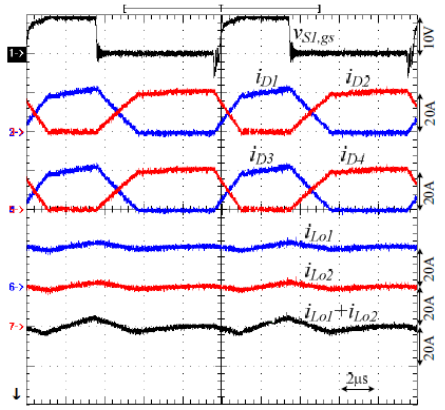


Fig.10 Measured waveforms of $v_{S1,gs}$, i_{D1}-i_{D4}, i_{Lo1} and i_{Lo2} at full load condition.

VI. Conclusion

This paper presents a new series APWM converter for high input voltage and high load current applications. Two half-bridge converters are connected in series to reduce the voltage stress of power switches at $V_{in}/2$. Thus, MOSFETs with 500V voltage stress can be used at 800V input voltage applications to achieve high switching frequency, low converter size and high circuit efficiency. Two series capacitors are connected at the AC terminals of two half-bridge converters in order to balance two input capacitor voltages in every switching cycle. Since APWM scheme is adopted to regulate output voltage, power switches can be turned on under ZVS within the desired load range and the magnetic flux can be reset. Two center-tapped rectifiers are used in the secondary side to share load current for high output current applications. Finally, experiments with 1kW prototype are provided to demonstrate the performance of the proposed converter.

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