出國報告（出國類別：其他-出席研討會發表論文）

出席「二〇一三年TENCON國際學術研討會」出國報告

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摘要

出席二〇一三年 IEEE-TENCON 國際會議，此行之主要目的為介紹國內電力電子之研究成果、學習國外電源轉換技術與專家學者討論未來研究趨勢。聆聽電力電子技術、能源控制、智慧控制、順滑模態控制、電動機研究趨勢與再生能源應用等最新研究與發展報告。研討會期間與研究領域相關的國外研究學者、專家相互討論能源轉換技術相關問題，藉以提升在電力電子研究方面的深度與廣度。研討會中，針對筆者發表兩種不同方法的諧振式直流對直流轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此兩種電路架構都具有流電壓及零電流切換技術，此兩種電路採用不同之控制方法，一種為變頻控制而另一種則為定頻控制方法，兩種控制方式完全不同，變頻方式適合用於窄輸入電壓範圍，定頻控制方式適合於寬輸入電壓之應用，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能。此次參加研討會獲得很多國外之研究成果，也詳細向國外學者介紹台灣之研究績效。

目次

一、 目的

參加二〇一三年IEEE-TENCON國際研討會之主要目的為1.發表電力電子實驗室近兩年來之研究成果，2.學習世界各研究學者與研究單位的研究方向，3.與國際學者廣泛討論各國之研究重點與科技趨勢方向，4.向各國介紹台灣在電源轉換器之研究現況。

二、 過程

二〇一三年IEEE-TENCON 國際研討會在中國/西安召開，會議時間自11月22日至11月25日。主辦單位為IEEE亞洲區協會，協辦單位為IEEE中國西安區分會，承辦單位為中國西北工業大學。TENCON國際學術研討會是每年舉辦一次的國際學術研討會，每年會議皆在亞洲國家舉辦(明年會議將在十月二十二至二十五日於泰國曼谷市舉辦)。此次研討會投稿篇數為六百四十五篇，投稿全文經兩位審稿者無記名審查，通過審查共有三百七十六篇論文於會議中發表。會議中安排有三場主題演講，會議內容共有四十個時段論文的口頭發表及2個時段海報張貼方式的論文發表。

22 日至 25 日參加各場次之論文發表會，筆者於研討會會中發表兩篇論文，題目為:

1. Parallel Resonant Converter with Flying Capacitor
2. Resonant Converter with Fixed Frequency Control

筆者論文中發表兩種不同方法的諧振式直流對直流轉換器架構，實現高效率及低損耗的電源供應器有深入之討論與答辯，此兩種電路架構都具有流電壓及零電流切換技術，此兩種電路採用不同之控制方法，一種為變頻控制而另一種則為定頻控制方法，兩種控制方式完全不同，變頻方式適合用於窄輸入電壓範圍,定頻控制方式適合於寬輸入電壓之應用，最後利用硬體電路實現來證明所提新型電力轉換器之實用性與優越性能。此兩篇文章獲得熱烈迴響。該會議為一有關之電機電子與應用之 IEEE 亞洲區國際研討會，會議內容包含電力電子，電力系統，IC 設計，影像處理，通信系統，控制工程等應用。

三、 心得

2013 年 IEEE- TENCON 為全世界有關電機電子相關研究方面重要會議之一。本次會議共有三百七十六篇論文，大陸是投稿篇數較多的國家，大陸近幾年在國際研討會的參與度相當積極且人數眾多，為提高台灣之學術地位及能見度，仍需國科會、教育部及各學術單位的努力。在本次的會議中可以看出論文廣度加大，在會議中能認識其他國家的人士，彼此能交換心得，對於開拓視野、提升研究品質有莫大的幫助。但是此次會議之人員安排及會議過程有點亂，與以往 TENCON 在其他國家舉辦之嚴謹度相比，今年在中國舉辦之 TENCON 會議是有需要改進之地方，茲將出席本次會議心得分

述如下：

1. 會中與各國專家學者交換意見，獲益良多。
2. 台灣學者在研究深度上表現很好。
3. 與中國、印度、日本及韓國學者在大會上廣泛互動與討論研究方向，作為將來合作之機會。
4. 此次會議中較多研究論文發表集中在太陽能及風能發電系統，利用高效能轉換器技術讓整體電源技術之效率提升，利用智慧型控制理論，增加實用性之產品應用。
5. 雲端電源技術之發展，在此次研討會中也是被討論主題之一。
6. 傳統電力穩定度控制也是主要論文發表重點，利用智慧型控制方法，讓電力控制更有效力。
7. 大型高瓦數電動機控制系統在研討會中也受到相當之重視。
8. 居家型照顧機器人有多篇論文發表。
9. 高效率電源器術在會議中討論踴躍，消費型電源技術有多篇在會議中發表，筆者在此方面之技術受到 IEEE-IE 及 PE 期刊副主編學者們肯定。

四、 建議事項

IEEE-TENCON 國際會議為 IEEE 亞洲區有關電機電子相關研究方面重要的國際會議，所發表的論文都相當嚴謹並具有創新性。會議中所發表的論文對工業升級及發展高科技所需的高效率電源及驅動系統之發展，均有相當的影響。由於參與類似的學術性會議非常重要，故有以下建議:

1. 中國學者出席國際研討會近幾年相當積極，人數超出台灣學者很多，台灣在此方面要多鼓勵國內學者出席介紹台灣教學研究成果。
2. 政府應對此領域之研究多作投資。
3. 鼓勵學者積極參與國際學術會議。

五、 附錄

1. 攜回 2013 年 IEEE- TENCON 光碟一片 。
2. 廠商資料及近一年相關的國際研討會資料。

大會會場

教師與研究生在會場

Parallel Resonant Converter with Flying Capacitor

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Abstract—**This paper presents a parallel resonant converter for high input voltage applications. In order to reduce the voltage stress of active switches, two half-bridge converters are connected in series at high voltage side. Flying capacitor is adopted between two series half-bridge converters to automatically balance two input capacitor voltages. Pulse frequency modulation scheme is adopted to regulate the output voltage at the desired voltage level. Since the resonant circuit at the switching frequency is operated at the inductive load, the input current of the resonant circuit is lagging to the fundamental input voltage. Active switches can be easier to turn on at zero voltage switching. Two resonant circuits connected in parallel are adopted to reduce the current stress of transformer windings and rectifier diodes at low voltage side. Interleaved pulse-width modulation is used to control two resonant circuits and to reduce the current ripple at the output side. Finally, experiments based on a laboratory prototype are presented to verify the effectiveness of the proposed converter.**

Keywords—**Resonant Converter, Flying Capacitor**

I. INTRODUCTION

Power converters with medium or high power level have been proposed and applied for many industry applications, such as fuel-cell power system [1], charge system [2] and ship power system [3]. For three-phase AC/DC power conversion systems, a three-phase 480V AC/DC converter with power factor correction (PFC) is normally adopted in the front stage to provide a stable DC bus voltage. This DC bus voltage may be equal to 800V. Power MOSFETs with high voltage stress, such as 900V voltage stress, will result in high turn-on resistance. Thus, the converters with high voltage MOSFETs have the serious conduction loss and low circuit efficiency. In order to overcome this limitation and decrease the converter size, three-level converters [4]-[6] with low voltage stress active switches and high switching frequency have been presented in DC/DC converters for high input voltage applications. Based on the neutral-point clamped diodes or flying capacitor, the voltage stress of active switches is clamped at $V_{in}/2$. However, two input split capacitor voltages maybe unbalanced and will increase the voltage stress of active switches beyond $V_{in}/2$. In [1] and [7], flying capacitor is adopted to the conventional three-level neutral point clamped converter to automatically balance two input capacitor voltages. Three-level converters with zero voltage switching (ZVS) [8]-[10] have been presented to reduce the switching losses and increase the circuit efficiency. Pulse-width modulation (PWM) schemes are adopted to generate the PWM signals for active switches and to regulate output voltage. However, the ZVS condition of active switches is related to the load condition and input voltage so that it is difficult to implement ZVS turn-on for all switches over the entire load range. In order to extend the ZVS condition over the whole load range, resonant converters [11]-[13] have been proposed to achieve ZVS turn-on over the wide load range and input voltage variation, no reverse recovery loss for rectifier diodes and high circuit efficiency. However, the ripple current at the output capacitor in resonant converter is higher than the output ripple current in the conventional half-bridge or full-bridge PWM converter. In order to limit the output ripple voltage in the desired ripple voltage specification, several capacitors are connected in parallel to reduce the resultant series equivalent resistance. Therefore, the large capacitance is normally adopted at the output side in the resonant converters.

A new parallel resonant converter is presented for high input voltage and high load current applications. Two circuit modules connected in parallel in order to share load power and reduce the current stress of all passive and active power components. These two circuit modules are controlled with the phase shift of one-fourth switching period in order to reduce the ripple current at the output capacitor. Thus, the size of output capacitor can be reduced. In each circuit module, two half-bridge converters are connected in series at the primary side to reduce the voltage stress of each active switch at $V_{in}/2$. Flying capacitor is connected between two half-bridge converters such that two input capacitor voltages can be automatically balanced in each switching cycle. Series-parallel resonant tank is adopted in each half-bridge converter to achieve ZVS turn-on for all switches over the entire load range. Finally, experiments were provided to verify the performance of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig. 1 gives the circuit configuration of the proposed converter for three-phase switching mode power supplies. The three-phase AC/DC converter with power factor correction is used in the front stage to reduce line current harmonics and provide a stable DC bus voltage for second stage DC/DC converter. The DC bus voltage is about 750V-800V for three-phase 480V utility input with power factor correction. The proposed parallel DC/DC converter with low voltage stress MOSFETs is adopted in the second stage for high load current applications. Two circuit modules are adopted in the proposed converter to share load current and reduce the current rating of active and passive components. The first circuit module includes C_{in1}-C_{in2}, C_{f1}, S_1-S_4, C_{S1}-C_{S4}, C_{r1}-C_{r2}, L_{r1}-L_{r2}, T_1-T_2, D_1-D_4 and C_o. In the same manner, the components of C_{in1}-C_{in2}, C_{f2}, S_5-S_8, C_{S5}-C_{S8}, C_{r3}-C_{r4}, L_{r3}-L_{r4}, T_3-T_4, D_5-D_5 and C_o are included in the circuit module 2. C_{in1} and C_{in2} are two input capacitances. C_{r1}-C_{r4} are the series resonant capacitances. L_{r1}-L_{r4} are the

series resonant inductances. L_{m1}-L_{m4} are the magnetizing inductances of transformers T_1-T_4, respectively. D_1-D_8 are the rectifier diodes and T_1-T_4 are the isolated transformers. C_{f1} and C_{f2} are the flying capacitances. Each circuit module includes two resonant converters with half-bridge converter leg. In circuit module 1, the first resonant converter includes the components of S_1, S_2, C_{r1}, L_{r1}, T_1, D_1, D_2 and C_o. The second resonant converter includes S_3, S_4, C_{r2}, L_{r2}, T_2, D_3, D_4 and C_o. C_o is the output capacitance. The primary sides of two resonant converters are connected in series in order to limit the voltage stress of each active switch at $V_{in}/2$. Active switches S_1 and S_3 have the same PWM waveforms. In the same manner, S_2 and S_4 have the same PWM signals. However, the PWM waveforms of S_1 and S_2 are complementary each other to avoid the short circuit in each half-bridge leg. In order to balance two input capacitor voltages v_{Cin1} and v_{Cin2}, C_{f1} is connected between the AC terminals b and c and C_{f2} is connected between the AC terminals f and g. If S_1 and S_3 are in the on-state and S_2 and S_4 are in the off-state, then $v_{Cf1}=v_{Cin1}$. On the other hand, $v_{Cf1}=v_{Cin2}$ if S_2 and S_4 are in the on-state. Since each active switch has the equal turn-on time, the flying capacitor voltage can be derived as $v_{Cf1}=v_{Cf2}=v_{Cin1}=v_{Cin2}=V_{in}/2$ and two capacitor voltages v_{Cin1} and v_{Cin2} are automatically balanced in each switching cycle. The frequency modulation scheme is used to regulate output voltage V_o. If the operated switching frequency is lower than the series resonant frequency, active switches S_1-S_8 are turned on at ZVS and rectifier diodes D_1-D_8 are turned off at ZCS. Thus, the switching losses of active switches are reduced and the reverse recovery problem of rectifier diodes is improved. In the proposed converter, each resonant converter supplies one-fourth of load power to output load for the medium/high load current applications.

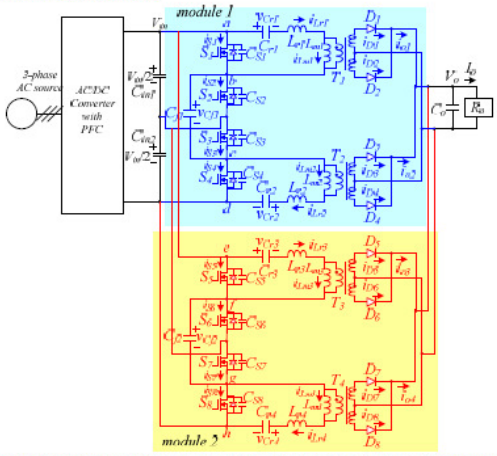


Fig. 1 Circuit configuration of the proposed converter with two circuit modules.

III. OPERATION PRINCIPLE

The circuit operations of the proposed converter are discussed with the following assumptions to simplify the system analysis. (1) Transformers T_1-T_4 are identical with the same turns ratio $n=n_p/n_{s1}=n_p/n_{s2}$ and same magnetizing inductances $L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_m$, (2) S_1-S_8 have the same output capacitance C_S, (3) $C_{in1}=C_{in2}$, (4) $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$, and (5) $L_{r1}=L_{r2}=L_{r3}=L_{r4}=L_r$. The main PWM waveforms of the proposed converter during one switching cycle are given in Fig. 2. Due to the on/off conditions of switches S_1-S_8 and rectifier diodes D_1-D_8, the proposed converter has twelve operation modes in one switching period. The corresponding equivalent circuits of twelve operation modes are shown in Fig. 3. Before time t_0, S_1-S_4 are all turned off in circuit module 1. i_{Lr1} and i_{Lr2} are positive and negative, respectively. Therefore, C_{S1} and C_{S3} are discharged and C_{S2} and C_{S4} are charged. Since $i_{Lr1}<i_{Lm1}$ and $i_{Lr2}>i_{Lm2}$, diodes D_2 and D_3 are in the on-state. In circuit module 2, S_6 and S_8 are in the on-state and diodes D_5 and D_8 are conducting. L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr3}(t_0+T_z)$, and L_{r4} and C_{r4} are resonant with the applied voltage $nV_o-v_{Cr4}(t_0+T_z)$.

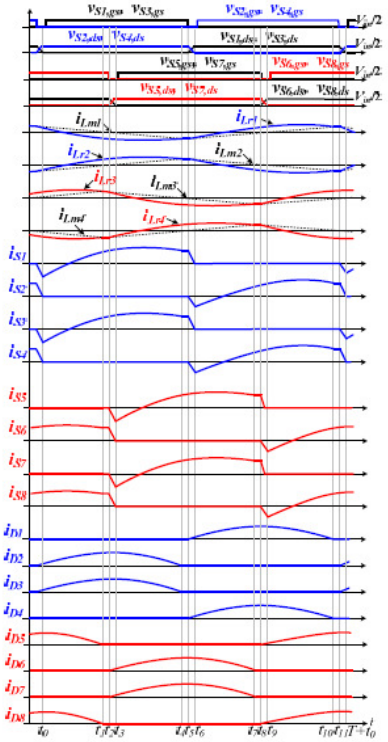


Fig. 2 Key waveforms of the proposed converter.

Mode 1 **[$t_0 \le t < t_1$]**: At t_0, capacitances C_{S1} and C_{S3} are discharged to zero voltage in circuit module 1. Since i_{Lr1} and i_{Lr2} are positive and negative, respectively, the anti-parallel diodes of S_1 and S_3 are conducting. Therefore, S_1 and S_3 can be turned on at this moment to achieve ZVS. In this mode, $i_{Lr1}<i_{Lm1}$ and $i_{Lr2}>i_{Lm2}$. Thus, D_2 and D_3 are conducting and the

magnetizing voltages v_{Lm1}=-nV_o and v_{Lm2}=nV_o. The magnetizing current i_{Lm1} decreases with the slope of -nV_o/L_m and i_{Lm2} increases with the slope of nV_o/L_m. In module 1, L_{r1} and C_{r1} are resonant with the applied voltage nV_o-$v_{Cr1}(t_0)$, L_{r2} and C_{r2} are resonant with the applied voltage $V_{in}/2$-nV_o-$v_{Cr2}(t_0)$, and the flying capacitor voltage v_{Cf1}=v_{Cin1}. In module 2, S_6 and S_8 are turned on and D_5 and D_8 are in the on-state. L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2$-nV_o-$v_{Cr3}(t_0)$, L_{r4} and C_{r4} are resonant with the applied voltage nV_o-$v_{Cr4}(t_0)$, and the flying capacitor voltage v_{Cf2}=v_{Cin2}.

The inductor currents i_{Lr1} and i_{Lr4} decrease and i_{Lr2} and i_{Lr3} increase in this mode.

Mode 2 **[$t_1 \le t < t_2$]:** At t_1, i_{Lr3}=i_{Lm3} and i_{Lr4}=i_{Lm4}. Thus, D_5-D_8 are in the off-state. Since S_6 and S_8 are still in the on-state, C_{r3}, L_{r3} and L_{m3} are resonant with the applied voltage $V_{in}/2$-$v_{Cr3}(t_1)$ and C_{r4}, L_{r4} and L_{m4} are resonant with the applied voltage -$v_{Cr4}(t_1)$ in circuit module 2. The operations of circuit module 1 in this mode are the same as the operation in mode 1.

Mode 3 **[$t_2 \le t < t_3$]:** At t_2, S_6 and S_8 are turned off. Since $i_{Lr3}(t_2)$ and $i_{Lr4}(t_2)$ are positive and negative, respectively, C_{S6} and C_{S8} are charged and C_{S5} and C_{S7} are discharged in this mode. Diodes D_6 and D_7 are conducting. Thus, the magnetizing voltages v_{Lm3}=-nV_o and v_{Lm4}=nV_o, and i_{Lm3} decreases and i_{Lm4} increases in this mode. If the energy stored in L_{r3} and L_{r4} is greater than the energy stored in C_{S5}-C_{S8}, then C_{S5} and C_{S7} can be discharged to zero voltage.

Mode 4 **[$t_3 \le t < t_4$]:** At t_3, C_{S5} and C_{S7} are discharged to zero voltage. Since $i_{Lr3}(t_3)$>0 and $i_{Lr4}(t_3)$<0, the anti-parallel diodes of S_5 and S_7 are conducting. Therefore, S_5 and S_7 can be turned on at this moment to achieve ZVS. Diodes D_6 and D_7 are conducting so that v_{Lm3}=-nV_o and v_{Lm4}=nV_o. In circuit module 2, L_{r3} and C_{r3} are resonant with the applied voltage nV_o-$v_{Cr3}(t_3)$ and L_{r4} and C_{r4} are resonant with the applied voltage $V_{in}/2$-nV_o-$v_{Cr4}(t_3)$.

Mode 5 **[$t_4 \le t < t_5$]:** At t_5, i_{Lm1}=i_{Lr1} and i_{Lm2}=i_{Lr2}. Thus, D_1-D_4 are all turned off. Components C_{r1}, L_{r1} and L_{m1} are resonant with the applied voltage -$v_{Cr1}(t_4)$ and C_{r2}, L_{r2} and L_{m2} are resonant with the applied voltage $V_{in}/2$-$v_{Cr2}(t_4)$.

Mode 6 **[$t_5 \le t < t_6$]:** At t_5, S_1 and S_3 are turned off and D_1 and D_4 are conducting. The magnetizing voltages v_{Lm1}=nV_o and v_{Lm2}=-nV_o. Since $i_{Lr1}(t_5)$<0 and $i_{Lr2}(t_5)$>0, C_{S1} and C_{S3} are charged and C_{S2} and C_{S4} are discharged. C_{S2} and C_{S4} can be discharged to zero voltage if the energy stored in L_{r1} and L_{r2} is greater than the energy stored in C_{S1}-C_{S4}. At t_6, v_{CS2}=v_{CS4}=0. The anti-parallel diodes of S_2 and S_4 are conducting. Then the operating modes in the first half of switching cycle are completed.

IV. Design Example and Experimental Results

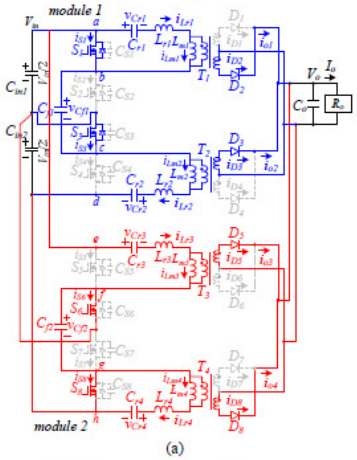
A laboratory prototype was implemented with the following specifications: V_{in}=750V-800V, V_o=24V, I_o=60A, and resonant frequency f_r=120kHz. Transformers T_1-T_4 were implemented with TDK EER-42 magnertic core with A_e=194mm^2. The primary and secondary winding turns of T_1-T_4 are 48 turns and 6 turns, respectively. The minimum and maximum voltage gains of resonant converter are given as:

$$G_{DC,\min} = \frac{4n(V_o + V_f)}{V_{in,\max}} = \frac{4\times(48/6)\times(24+0.8)}{800} \approx 0.992 \quad (1)$$

$$G_{DC,\max} = \frac{4n(V_o + V_f)}{V_{in,\min}} = \frac{4\times(48/6)\times(24+0.8)}{750} = 1.058 \quad (2)$$

where V_f is the voltage drop on diodes D_1-D_8. At full load, the AC equivalent resistances $R_{ac,T1}$-$R_{ac,T4}$ are given as:

$$R_{ac,T1} = R_{ac,T2} = R_{ac,T3} = R_{ac,T4} = 32n^2 R_o / \pi^2 \approx 83\Omega \quad (3)$$



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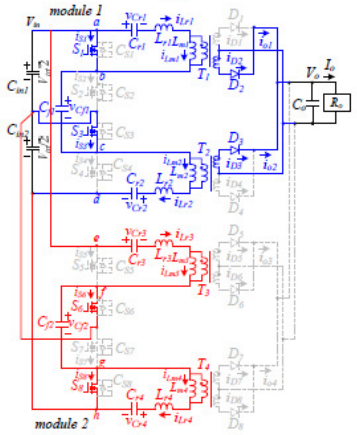

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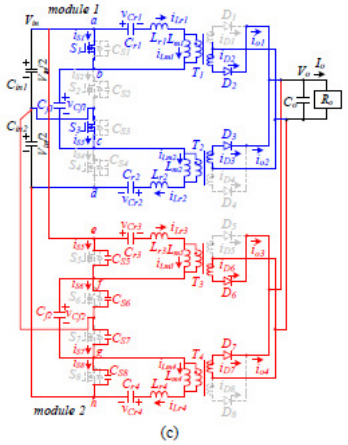
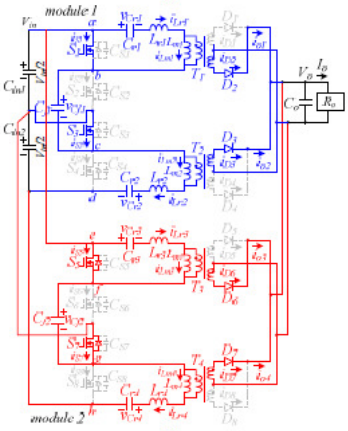
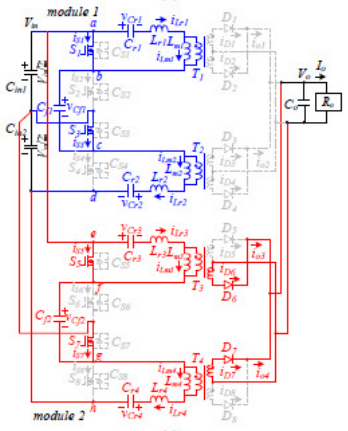


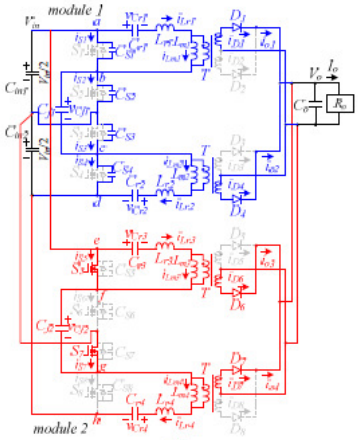
(c)



(d)



(e)



(f)

Fig. 3 Operation modes of the proposed converter during the first half switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6.

In this prototype, the inductance ratio k=L_{r1}/L_{m1} is selected as 1/8 and the quality factor Q at full load is selected as 0.3. Thus, the AC voltage gain of the proposed converter at no load condition (Q=0) is obtained as $|G_{AC}(f)|_{Q=0,f_s=\infty} \approx 1/(1+k) = 0.889$. The minimum DC voltage gain $G_{DC,min}$ of the proposed converter is 0.992 and greater than the AC voltage gain at no load condition. Thus, the output voltage at no load condition can be controlled. From the given series resonant frequency f_r, the selected quality factor Q, the inductance ratio k and the AC equivalent resistance $R_{ac,T1}$, the series resonant inductances L_{r1}-L_{r4}, the magnetizing inductances L_{m1}-L_{m4} and the resonant capacitances C_{r1}-C_{r4} can be obtained as:

$$L_{r1} = L_{r2} = L_{r3} = L_{r4} = \frac{QR_{ac,T1}}{2\pi f_r} = \frac{0.3\times 83}{2\pi \times 120\times 10^3} \approx 33\mu H \quad (4)$$

$$L_{m1} = L_{m2} = L_{m3} = L_{m4} = L_{r1}/k = \frac{33\mu H}{1/8} \approx 264\mu H \quad (5)$$

$$C_{r1} = C_{r2} = C_{r3} = C_{r4} = \frac{1}{4\pi^2 L_{r1} f_r^2} \approx 53nF \quad (6)$$

Since two flying capacitors C_{f1} and C_{f2} are used to balance two input capacitor voltages V_{Cin1} and V_{Cin2}, the voltage stresses of S_1-S_8 can be limited at $V_{in,max}/2$.

$$v_{S1,stress} = V_{in,\max}/2 = 400V \quad (7)$$

The MOSFETs IRFP460 with 500V voltage stress and 20A current stress are adopted for active switches S_1-S_8. The voltage stress and average current of rectifier diodes D_1-D_8 are obtained as:

$$v_{D1,stress} = 2(V_o + V_f) = 2\times(24+0.8) = 49.6V \quad (8)$$

$$i_{D1,av} = I_{o,\max}/8 = 60/8 = 7.5A \quad (9)$$

The fast recovery diodes 30CPQ150 with 150V voltage stress, 30A current stress and 0.8V voltage drop are used for

diodes D_1-D_8. The input capacitances C_{in1} and C_{in2} are 680nF/450V, the flying capacitances C_{f1} and C_{f2} are 680nF/630V, and the output capacitance C_o is 3000μF/100V.

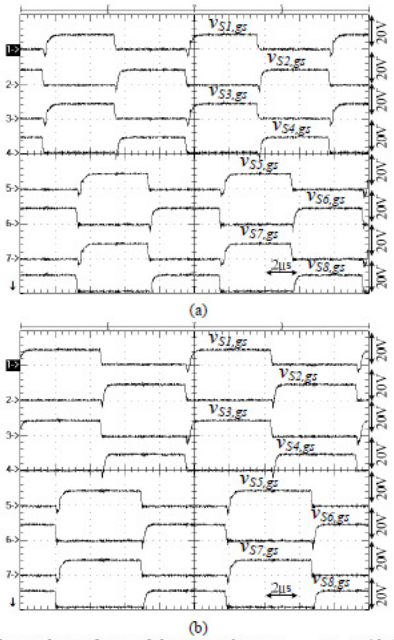


Fig. 4 Measured waveforms of the gate voltages $v_{S1,gs}$ - $v_{S8,gs}$ with V_{in}=800V and (a) 25% load (b) full load.

A laboratory prototype with the circuit parameters derived in the previous section was implemented and tested to verify the effectiveness of the proposed converter. The measured gate voltages of S_1-S_8 with input voltage V_{in}=800V and 25% load and full load are shown in Fig. 4. The PWM signals of S_5-S_8 are phase-shifted one-fourth of switching period with respectively to PWM signals of S_1-S_4, respectively. Fig. 5 gives the measured results of gate voltage, drain voltage and drain current of switch S_1 at 5% load. Before switch S_1 is turned on, the drain current is negative to discharge the drain-to-source capacitor. Thus, switch S_1 can be turned on under ZVS when drain voltage is decreased to zero voltage. Fig. 6 illustrates the measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and V_{in}=800V. Two input capacitor voltages and two flying capacitor voltages are all balanced at 400V. Fig. 7 gives the measured waveforms of inductor currents i_{Lr1} - i_{Lr4} at full load. Four inductor currents i_{Lr1} - i_{Lr4} are balanced. Fig. 8 shows the measured waveforms of four resonant capacitor voltages v_{Cr1} - v_{Cr4} at full load condition. Fig. 9 gives the test results of the rectifier output currents i_{o1} - i_{o4} at full load condition. The rectifier output currents i_{o1} - i_{o4} are almost balanced. Fig. 10 shows the measured circuit efficiencies of the proposed converter at different load conditions.

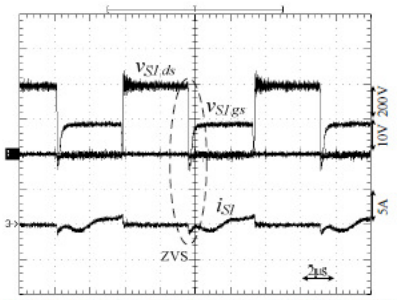


Fig. 5 Experimental results of gate voltage, drain voltage and drain current of switch S_1 at 5% load with V_{in}=800V.

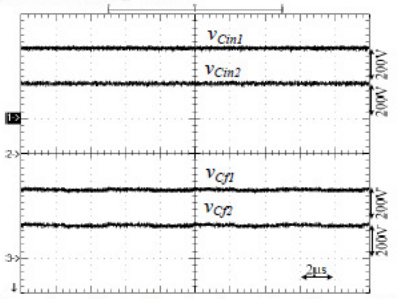


Fig. 6 Measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and V_{in}=800V.

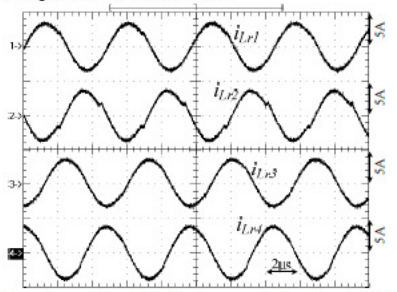


Fig. 7 Measured waveforms of inductor currents i_{Lr1} - i_{Lr4} at full load with V_{in}=800V.

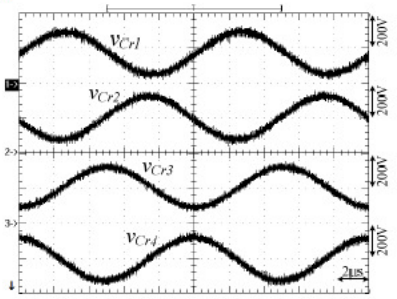


Fig. 9 Measured waveforms of resonant capacitor voltages v_{Cr1} - v_{Cr4} at full load with V_{in}=800V.

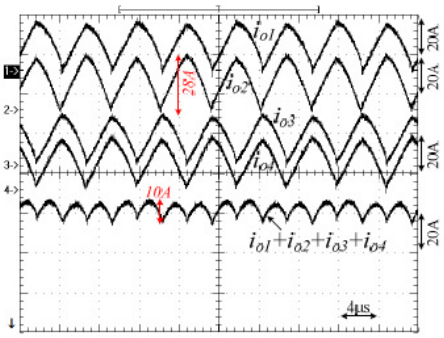


Fig. 10 Measured waveforms of the center-tapped rectifier output currents i_{o1}–i_{o4} at full load with V_{in}=800V.

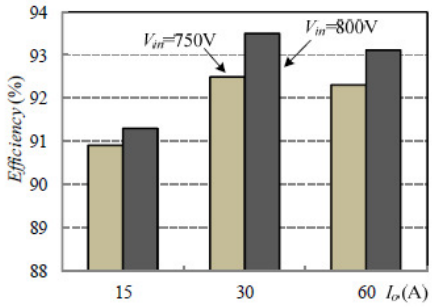


Fig. 11 Measured efficiencies of the proposed converter at different load conditions.

V. CONCLUSION

A new parallel resonant converter is presented for high input voltage and high load current applications. The main functions of the proposed converter are low voltage stress of MOSFETs, ZVS turn-on for all MOSFETs, no reverse recovery loss on rectifier diodes, low current rating of transformer windings and less ripple current on output capacitor. Two resonant circuit modules with interleaved PWM scheme are adopted in the proposed converter to reduce the current stress of active and passive components and reduce the ripple current at output side. In each circuit module, one flying capacitor is added between two half-bridge legs to balance two input capacitor voltages. Two resonant converters are connected in series in order to reduce the voltage stress of each MOSFET at $V_{in}/2$. The pulse frequency modulation scheme is used to regulate output voltage. The switching frequency is controlled to be less than the series resonant frequency so that MOSFETs can be turned on at ZVS and rectifier diodes can be turned off at ZCS. The switching loss of MOSFETs is reduced and the reverse recovery loss of rectifier diodes is overcome. Finally, experiments based on a laboratory prototype are provided to verify the effectiveness of the proposed converter.

ACKNOWLEDGMENT

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Resonant Converter with Fixed Frequency Control

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***Abstract*—This paper presents a soft switching DC/DC converter for renewable energy conversion applications. Phase-shifted full-bridge converter with a series resonant tank is adopted to achieve zero voltage switching (ZVS) turn-on for power switches and zero current switching (ZCS) for rectifier diodes within nearly entire load range. Thus the switching losses of power switches and reverse recovery current of rectifier diodes are improved and the circuit efficiency is improved. In order to overcome the drawback of a wide range of switching frequency in the conventional series resonant converters, fixed frequency pulse-width modulation is adopted to regulate the output voltage. In order to reduce and balance the current rating of transformer primary windings for low input voltage applications, the primary and secondary turns of transformers are connected in parallel and series respectively. Full-bridge diode rectifier is adopted at the secondary side to reduce the voltage rating of rectifier diodes for high output voltage applications. Based on the resonant behavior by the output capacitances of MOSFETs and the resonant inductance, all power switches are turned on at ZVS. Finally, experiments based on a scale down prototype are provided to verify the effectiveness of the proposed converter.**

***Keywords*—Resonant Converter, PWM**

I. INTRODUCTION

New clean energies have been developed in order to reduce the environmental pollution resulting from greenhouse gas emissions from fossil fuel based power generation. The Environment Protection Agency (EPA) and Climate Saver Computing Initiative (CSCI) have proposed efficiency requirements for modern power supply units. If power semiconductors, magnetic components and passive components with low power losses are adopted, then power converters with high circuit efficiency can be achieved. However, the cost of the power circuits is very expensive. Therefore, it is a better way to increase the circuit efficiency using the soft switching technique to the power converters. Soft switching techniques, such as asymmetric pulse-width modulation (PWM) techniques [1]-[2], active-clamping converters [3]-[6] and phase-shift PWM converters [7]-[8], have been proposed for the past twenty years to reduce switching losses of MOSFETs and improve the reverse recovery loss on rectifier diodes. However, the zero voltage switching (ZVS) effect of these approaches is limited to specific input voltage ranges or load conditions. Thus, it is difficult to design soft switching converters with wide load ranges. Resonant converters in [9]-[14] with variable switching frequency to regulate the output voltage have been proposed with the advantages of ZVS or zero current switching (ZCS) for nearly the entire load and input voltage range. However, the resonant converter has a wide range of switching frequency from light load to full load. Therefore, the magnetic components in the resonant converter are not easy to design at the optimal point. It is better that the converter has the ZVS and ZCS functions of resonant converter and operates at a duty cycle control without a wide range of frequency variation.

This paper presents a full-bridge series resonant converter with duty cycle control to have the following advantages: 1) power switches are turned on at ZVS from nearly entire load range; 2) the rectifier diodes are turned off at ZCS without reverse recovery loss and the voltage stress of rectifier diodes is equal to output voltage; and 3) constant switching frequency is adopted to regulate output voltage. Since the input impedance of the resonant tank is an inductive load at the operating switching frequency, the resonant current lags the fundamental input voltage applied to the resonant network. Thus, power switches can be turned on at ZVS within nearly from zero to full load. The operating switching frequency is less than the series resonant frequency such that rectifier diodes are turned off at ZCS with wide input voltage range. The switching losses on power switches and reverse recovery problem on rectifier diodes can be reduced. At the low voltage side, two transformers are used to reduce the size of the magnetic core and lessen the current stress on the primary windings. At high voltage side, the secondary windings of two transformers are connected in series in order to balance the transformer primary currents, to share the input current, and to reduce the secondary winding turns. The adopted converter can be used in low and medium power converters such as solar power conversion, fuel cell power conversion and battery discharger in UPS system. Finally, Experiments based on a 500W prototype are provided to verify the operation principle of the proposed converter.

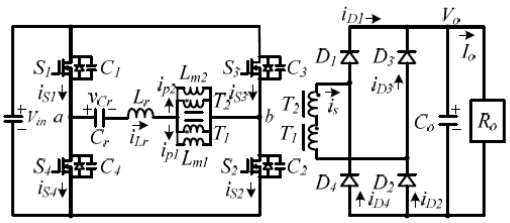


Fig. 1 Circuit configuration of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig. 1 shows the circuit configuration of the proposed converter. V_{in} and V_o are the input voltage and output voltage respectively. S_1-S_4 are MOSFETs and the voltage stresses of S_1-S_4 are equal to V_{in}. C_1-C_4 are the output capacitances of MOSFETs S_1-S_4, respectively. C_r is the series resonant

capacitor and L_r is the series resonant inductor. L_{m1} and L_{m2} are the magnetizing inductances of the transformers T_1 and T_2, respectively. D_1-D_4 are the rectifier diodes. C_o is the output filter capacitor and R_o is the load resistance. The series resonant converter with duty cycle control is proposed in this paper. Three-level PWM waveform is generated on the AC side voltage v_{ab}. Switches S_1-S_4 are phase-shift controlled. S_1 and S_4 are the leading switches, and S_2 and S_3 are the lagging switches. Since the capacitor C_r is in series with the power path, the flux balancing can be automatically achieved. The primary sides of two transformers are connected in parallel to reduce the current stresses of transformer primary windings and the size of the magnetic cores for high input current applications. The secondary windings of two transformers are connected in series to reduce the winding turns for high output voltage applications and to balance the primary winding currents. Based on the resonant behavior during the transition interval, power switches are all turned on with ZVS. Since the series resonant frequency is higher than the switching frequency, the rectifier diode can be turned off with ZCS such that there is no reverse recovery loss on the rectifier diodes.

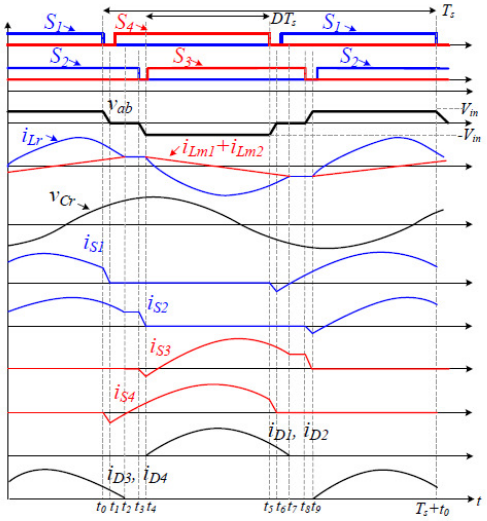


Fig. 2 Key waveforms of the proposed converter.

III. Operation Principle

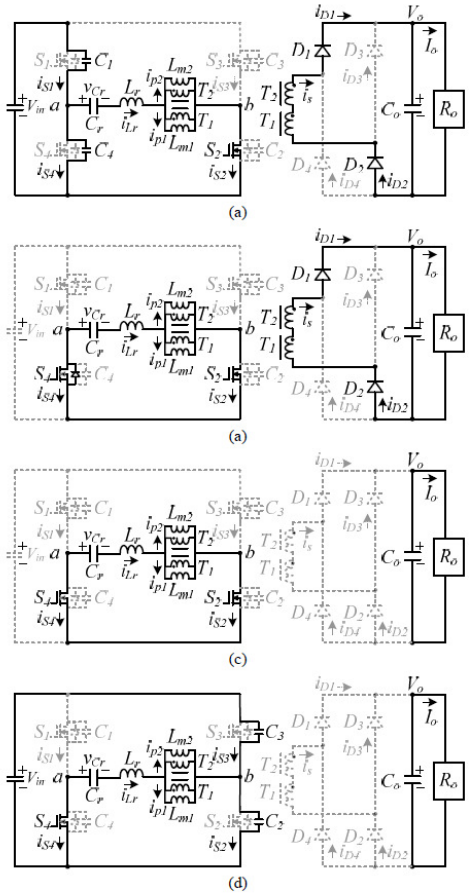
The main PWM waveforms of the proposed converter in a switching period are shown in Fig. 2. The PWM signals of S_2 and S_3 are phase-shifted with respective to the PWM signals of S_1 and S_4. The following assumptions are made to simplify the circuit analysis.

(1) MOSFETs S_1-S_4 and diodes D_1-D_4 are ideal.
(2) $L_{m1}=L_{m2}=L_m$ and $L_r<L_m$.
(3) Turns ratio of transformers T_1 and T_2 is $n=n_p/n_s$.
(4) $C_1=C_2=C_3=C_4=C_{oss}$ and $C_r >>C_{oss}$.
(5) C_o is large enough and V_o is a constant output voltage.

Based on the on/off states of S_1-S_4 and D_1-D_4, the adopted converter has ten operation modes in a switching period. Fig. 3 shows the equivalent circuits in a switching period. Prior to t_0, power semiconductors S_1, S_2, D_1 and D_2 are conducting and $i_{Lr}>0$.

***Mode 1* [$t_0 \le t < t_1$]:** At t_0, S_1 is turned off. Since $i_{Lr}(t_0)>0$, C_1 and C_4 are charged and discharged respectively. v_{C1} rises and v_{C4} decays linearly. S_1 is turned off with zero voltage due to C_1 and C_4. If the energy stored in L_r is greater than the energy stored in C_1 and C_4, then v_{C4} can be discharged to zero at t_1. D_1 and D_2 still conduct, and i_{Lm1} and i_{Lm2} keep increasing linearly.

***Mode 2* [$t_1 \le t < t_2$]:** At t_1, v_{C4} declines to zero and $v_{C1}=V_{in}$. Since $i_{Lr}(t_1)>0$, the anti-parallel diode of S_4 is conducting. Thus, S_4 can be turned on with zero voltage. The AC terminal voltages $v_{ab}=0$. Since $i_{Lr}>i_{Lm1}+i_{Lm2}$, D_1 and D_2 keep conducting in this mode. The magnetizing inductor voltages $v_{Lm1}=v_{Lm2}=nV_o/2$. The magnetizing currents i_{Lm1} and i_{Lm2} keep increasing linearly. L_r and C_r are resonant with the applied voltage $-nV_o/2$ and i_{Lr} decreases. Thus, i_{D1} and i_{D2} decrease in this mode.



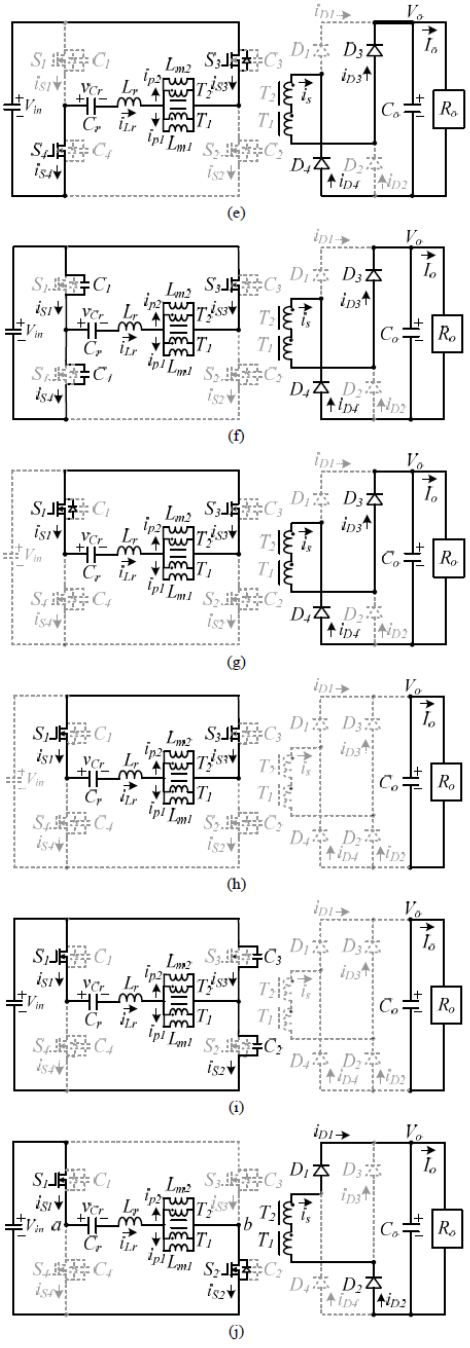


Fig. 3 Operation modes of the proposed converter in a switching period (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10.

Mode 3 **[$t_2 \le t < t_3$]:** At t_2, $i_{Lr}=i_{Lm1}+i_{Lm2}$ such that i_{D1} and i_{D2} are decreased to zero. Therefore, D_1 and D_2 are turned off with ZCS and there is no reverse recovery loss. C_r, L_r, L_{m1} and L_{m2} are resonant in this mode.
Since $L_m >> L_r$, i_{Lr} is approximately unchanged in this mode.

Mode 4 **[$t_3 \le t < t_4$]:** At t_3, S_2 is turned off. Since $i_{Lr}(t_3)>0$, v_{C2} rises and v_{C3} decays linearly. S_2 is turned off with zero voltage due to C_2 and C_3. If the energy stored in L_r, L_{m1} and L_{m2} is greater than the energy stored in C_2 and C_3, then v_{C3} can be discharged to zero at t_4. At t_5, v_{C3} is decreased to zero voltage and the anti-parallel diode of S_3 is conducting.

Mode 5 **[$t_4 \le t < t_5$]:** At t_4, v_{C3} decreased to zero voltage. Since $i_{Lr}(t_4)>0$, the anti-parallel diode of S_3 is conducting and S_3 is turned on at this moment to achieve ZVS. The AC terminal voltage $v_{ab}=-V_{in}$. Since the primary voltages of T_1 and T_2 are negative, D_3 and D_4 are conducting. The magnetizing inductor voltages $v_{Lm1}=v_{Lm2}=-nV_o/2$ and i_{Lm1} and i_{Lm2} decrease linearly. L_r and C_r are resonant with the applied voltage $-V_{in}+nV_o/2$ and i_{Lr} decreases in this mode. Power is delivered from input voltage V_{in} to output load R_o through the resonant tank and diodes D_3 and D_4 in this mode.

Mode 6 **[$t_5 \le t < t_6$]:** At t_5, S_4 is turned off. Since $i_{Lr}(t_5)<0$, C_1 and C_4 are discharged and charged respectively. v_{C4} rises and v_{C1} decays linearly. S_4 is turned off with zero voltage due to C_1 and C_4. If the energy stored in L_r at time t_5 is greater than the energy needed to charge C_4 from zero voltage to V_{in} and to discharge C_1 from V_{in} to zero voltage, then C_1 can be decayed to zero voltage at t_6. D_3 and D_4 still conduct, and i_{Lm1} and i_{Lm2} keep decreasing linearly.

Mode 7 **[$t_6 \le t < t_7$]:** At t_6, v_{C1} declines to zero voltage and $v_{C4}=V_{in}$. Since $i_{Lr}(t_6)<0$, the anti-parallel diode of S_1 is conducting. Therefore, S_1 is turned on at zero voltage and the AC terminal voltages $v_{ab}=0$. Since $i_{Lr}<i_{Lm1}+i_{Lm2}$, D_3 and D_4 keep conducting in this mode and $v_{Lm1}=v_{Lm2}=-nV_o/2$. Thus, the magnetizing currents i_{Lm1} and i_{Lm2} keep decreasing. L_r and C_r are resonant with the applied voltage $nV_o/2$ and i_{Lr} increases. Thus, i_{D3} and i_{D4} decrease in this mode.

Mode 8 **[$t_7 \le t < t_8$]:** At t_7, $i_{Lr}=i_{Lm1}+i_{Lm2}$ such that i_{D3} and i_{D4} are equal to zero and D_3 and D_4 are turned off with ZCS. Thus, there is no reverse recovery loss on D_3 and D_4. C_r, L_r, L_{m1} and L_{m2} are resonant in this mode.

Mode 9 **[$t_8 \le t < t_9$]:** At t_8, S_3 is turned off. Since $i_{Lr}(t_8)<0$, v_{C3} rises from zero voltage and v_{C2} decays from V_{in}. S_3 is turned off with zero voltage due to C_2 and C_3. If the energy stored in L_r, L_{m1} and L_{m2} is greater than the energy needed to discharge C_2 from V_{in} to zero and to charge C_3 from zero voltage to V_{in}, then S_2 can be turned on with zero voltage. At t_9, v_{C2} is decreased to zero voltage and the anti-parallel diode of S_2 is conducting.

Mode 10 **[$t_9 \le t < T_s+t_0$]:** At t_9, v_{C2} declined to zero voltage. Since $i_{Lr}(t_9)<0$, the anti-parallel diode of S_2 is conducting and S_2 can be turned on with zero voltage. The AC terminal voltage $v_{ab}=V_{in}$. The primary voltages of T_1 and T_2 are positive. Thus, D_1 and D_2 are conducting in the secondary side. The

magnetizing inductor voltages v_{Lm1}=v_{Lm2}=nV_o/2 and the magnetizing currents i_{Lm1} and i_{Lm2} increase linearly. L_r and C_r are resonant with the applied voltage V_{in}-nV_o/2. i_{Lr} increases in this mode. Power is delivered from input voltage V_{in} to output load R_o through the resonant tank and diodes D_1 and D_2 in this mode. At time T_s+t_0, S_1 is turned off. Then, the operations of the adopted converter in a switching period are completed.

IV. Circuit Characteristics

In the operation modes 2, 5, 7 and 10 the adopted converter is resonant at the series resonant frequency $f_r = 1/2\pi\sqrt{L_rC_r}$. In modes 3 and 8, the converter is resonant by L_r, L_m/2 and C_r with resonant frequency $f_m = 1/2\pi\sqrt{(L_r + L_m/2)C_r}$. Based on the fundamental frequency analysis of the conventional series resonant converter, the AC voltage gain of the resonant tank related to the switching frequency is derived as:

$$|G_{ac}(f)| = \frac{V_{Lm1}}{V_{ab,f}} = \frac{1}{\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2 + Q^2(\frac{f_s}{f_r} - \frac{f_r}{f_s})^2}} \quad (1)$$

Where k=$2L_r/L_m$, , $R_{ac} = 4n^2R_o/\pi^2$, $f_r = 1/2\pi\sqrt{L_rC_r}$, $Q = 2Z_o/R_{ac} = 2\sqrt{L_r/C_r}/R_{ac}$ and f_s is the switching frequency. The maximum DC voltage gain of the proposed converter is expressed as

$$G_{dc,\max} = \frac{n(V_o + 2V_D)}{2V_{in,\min}} \quad (2)$$

where V_D is the voltage drop on D_1-D_4. If the duty ratio of power switches is less than 0.5, then the voltage gain of the proposed converter is less than maximum DC gain $G_{dc,max}$. Since the proposed converter with duty cycle control is depended on the initial resonant inductor current and resonant capacitor voltage, it is not easy to obtain the voltage conversion ratio at steady state. Therefore, the voltage conversion ratio of the adopted series resonant converter with duty cycle control is a function of output power and duty ratio. If the inductor ratio k, Q, f_s, f_r and $V_{in,min}$ are given, then the turns ratio of transformers can be obtained from (1) and (2). Since the proposed converter is operated at f_s<f_r, the magnetizing current variation is equal to

$$\Delta i_{Lm1} = \frac{n(V_o + 2V_D)}{4L_m f_r} = 2I_m \quad (3)$$

where I_m is the peak current of magnetizing inductor. Thus, I_m can be further expressed as:

$$I_m = \frac{n(V_o + 2V_D)}{8L_m f_r} \quad (4)$$

The voltage stress of switches S_1-S_4 is equal to V_{in} in the adopted converter. In the full-bridge converter, the lagging switches are more difficult to achieve ZVS than the leading switches. To implement the ZVS turn-on of the lagging switches, the energy stored in L_r and L_m/2 in modes 4 and 9 must be greater than the energy stored on capacitors C_2 and C_3.

$$(L_r + L_m/2)I_m^2 = (L_r + L_m/2)[\frac{n(V_o + 2V_D)}{8L_m f_r}]^2 \geq 2C_{oss}V_{in}^2 \quad (5)$$

If the equation (5) is satisfied, then all power switches can be turned on under ZVS.

V. Design Example and Experimental Results

The adopted converter was implemented with the following specifications: V_{in}=44V~52V, V_o=400V, $P_{o,rated}$=500W, series resonant frequency f_r=130kHz, switching frequency is f_s=110kHz, k=0.25 and Q=0.6. Based on (1) and the given k, the AC voltage gain versus the variable switching frequency is drawn in Fig. 4. Since the selected frequency ratio f_s/f_r=110/130, the AC voltage gain at 110kHz switching frequency and Q=0.6 can be obtained as G_{ac}(110/130)=1.09=$G_{dc,max}$. From (2), the necessary turns ratio of transformers T_1 and T_2 are expressed as:

$$n = \frac{2V_{in,\min}G_{dc,\max}}{V_o + 2V_D} = \frac{2\times44\times1.09}{400+2\times1.7} \approx 0.238 \quad (6)$$

where V_D is the voltage drop on D_1-D_4. The primary and secondary winding turns of T_1 and T_2 are 8 turns and 33 turns respectively. The AC equivalent resistance R_{ac} at full load is obtained as:

$$R_{ac} = \frac{4n^2}{\pi^2}R_{o,rated} = \frac{4\times(8/33)^2}{\pi^2}\times\frac{400}{1.25} \approx 7.62\Omega \quad (7)$$

Since the selected series resonant frequency f_r is 130kHz, we can obtain the required series inductance.

$$L_r = \frac{QR_{ac}}{4\pi f_r} = \frac{0.6\times7.62}{4\pi\times130000} \approx 2.8\mu H \quad (8)$$

Since we select k=$2L_r/L_m$=1/4, the magnetizing inductances of T_1 and T_2 are given as:

$$L_m = 2L_r/k = \frac{2\times2.8\mu H}{1/4} \approx 22.4\mu H \quad (9)$$

The series resonant capacitance C_r is given as:

$$C_r = \frac{1}{4\pi^2L_rf_r^2} = \frac{1}{4\pi^2\times2.8\times10^{-6}\times(130000)^2} \approx 0.535\mu F \quad (10)$$

The actual series resonant capacitance C_r in the prototype circuit is 0.55μF. Thus the actual series resonant frequency is $f_r = 1/2\pi\sqrt{L_rC_r} \approx 128kHz$. The voltage stress, rms current and average current of rectifier diodes D_1-D_4 are given as:

$$v_{D,\max} = V_o + V_D = 400 + 1.7 = 401.7V,$$
$$i_{D,rms} = \pi I_{o,\max}/4 \approx 1.34A,$$
$$i_{D,av} = I_o/2 = 1.25/2 = 0.625A \quad (11)$$

Thus, the fast recovery diodes BR506 with 600V voltage stress, 5A current stress and 1.7V voltage drop are used for rectifier diodes D_1-D_4. The voltage stress of power switches S_1-S_4 are given as:

$$v_{S1,\max} = V_{in,\max} = 52V \quad (12)$$

The MOSFETs IRFP264*4 with 250V voltage stress and 38A current stress are used for power switches S_1-S_4. Since C_{oss} of the IRFP264 is 870pF at 25V, the equivalent output capacitance C_{oss} at the maximum input voltage 52V is given as:

$$C_{oss,52} \approx \frac{4}{3} C_{oss,25} \sqrt{\frac{25}{v_{S1,ds}}} = \frac{4}{3} \times 870 \times \sqrt{\frac{25}{52}} \approx 804 pF \qquad (13)$$

With the derived circuit parameters L_r, L_m and n, equation (5) is stratified. And switches S_1-S_4 can realize ZVS in the entire load range in the theoretical analysis. The output capacitance C_o is 680μF/450V. The phase-shift PWM IC UC3895 is used to generate PWM signals for S_1-S_4 and to regulate the output voltage at the desire voltage level.

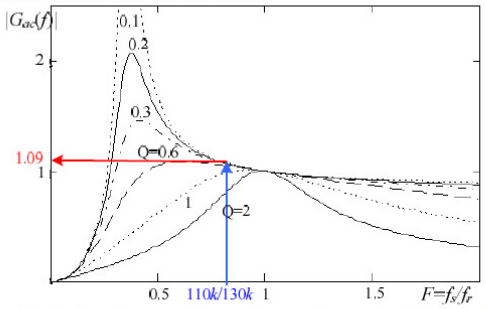


Fig. 4 Typical ac gain curves of proposed resonant converter with $V_{in,min}$=44V and f_s/f_r=110kHz/130kHz.

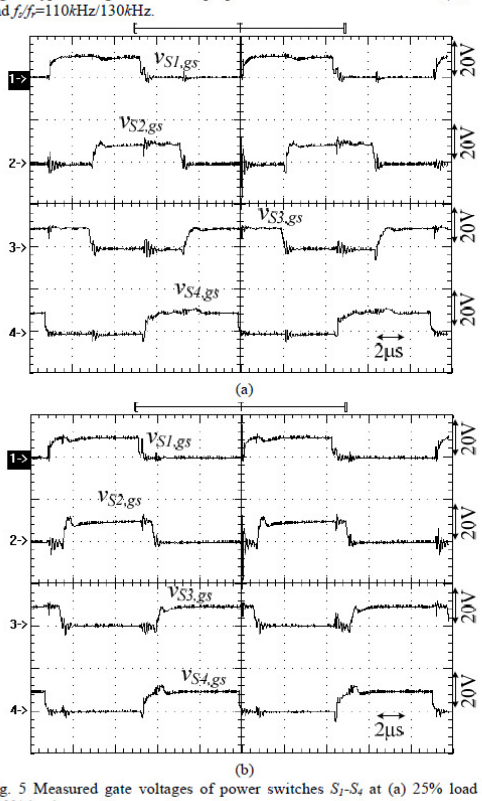


Fig. 5 Measured gate voltages of power switches S_1-S_4 at (a) 25% load (b) 100% load.

Experimental results of a laboratory prototype are provided to verify the effectiveness of the proposed converter. Fig. 5 shows the measured waveforms of the PWM signals of S_1-S_4 at 25% load and full load conditions. Switches S_2 and S_3 are phase-shifted with respective to switches S_1 and S_4 respectively. Fig. 6 shows the measured gate voltage, drain voltage and switch current of switches S_1 and S_2 at 25% load and full load conditions. Before S_1 and S_2 are turned on, the drain-to-source voltages have been decreased to zero and switch currents are negative. Thus, S_1 and S_2 are all turned on with ZVS from 25% to 100% loads. It is also clear in Fig. 6 that the voltage stress of S_1 and S_2 is equal to V_{in}. In the same manner, we can expect that the switches S_3 and S_4 are also turned on with ZVS from 25% load to 100% load. Fig. 7 gives the measured AC terminal voltage v_{ab}, resonant capacitor voltage v_{Cr} and resonant inductor current i_{Lr} at full load condition. Fig. 8 illustrates the measured waveforms of the switch currents i_{S1}-i_{S4} and resonant inductor current i_{Lr} at full load condition. If S_1 and S_2 are both in the on-state, then the inductor current i_{Lr} decreases. On the other hand, the inductor current i_{Lr1} decreases if S_3 and S_4 are both in the on-state. Fig. 9 shows the measured waveforms of the resonant inductor current i_{Lr} and diode currents i_{D1}-i_{D4} at full load condition. It is clear than diodes D_1-D_4 all turned off at ZCS and there is no reverse recovery loss on the rectifier diodes.

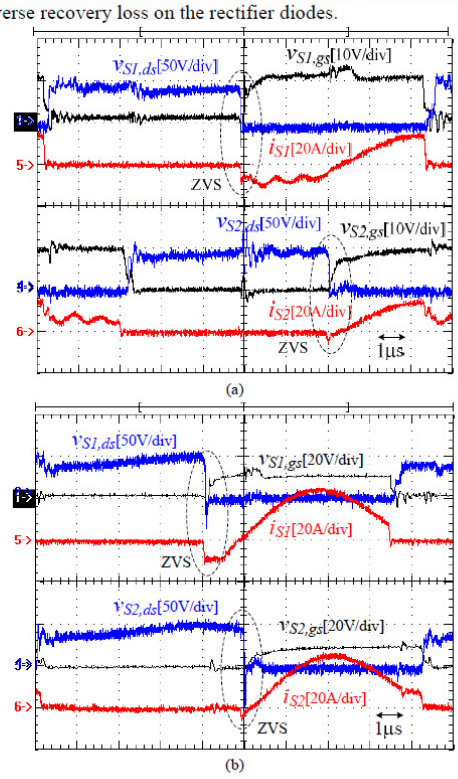


Fig. 6 Measured gate voltage, drain voltage and switch current of S_1 and S_2 at (a) 25% load (b) 100% load.

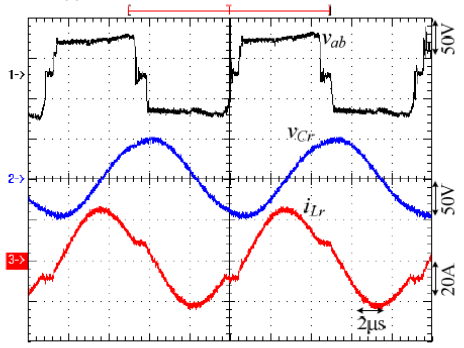


Fig. 7 Measured waveforms of the AC terminal voltage v_{ab}, resonant capacitor voltage v_{Cr} and resonant inductor current i_{Lr} at full load condition.

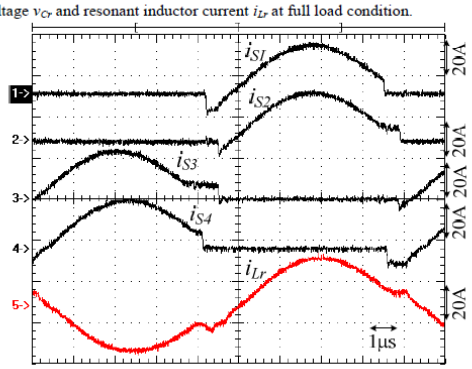


Fig. 8 Measured waveforms of the switch currents i_{S1}-i_{S4} and resonant inductor current i_{Lr} at full load condition.

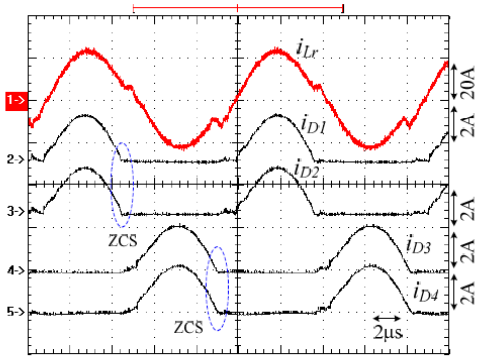


Fig. 9 Measured waveforms of the resonant inductor current i_{Lr} and diode currents i_{D1}-i_{D4} at full load condition.

VI. Conclusion

Phase-Shift full-bridge series resonant converter is presented in this paper for low input voltage applications such as battery discharge circuit and renewable DC/DC converter. Instead of the variable switching frequency in the conventional series resonant converter, the fixed switching with duty cycle control is adopted in the proposed converter to regulate the output voltage. Based on the series resonant behavior, all switches are turned on at ZVS. The operating switching frequency is lower than the series resonant frequency such that the rectifier diodes are all turned off at ZCS and there is no reverse recovery loss on the rectifier diodes. Thus the switching losses on power semiconductors are reduced. Two transformers are connected in parallel at the primary side to reduce the current rating of the primary windings and connected in series at the secondary side to reduce the secondary winding turns. Bridge diode rectifier is used at the secondary side to reduce the secondary winding turns for high output voltage applications. Finally, experiments based on a laboratory prototype are provided to verify the effectiveness of the converter.

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