出國報告(出國類別:國際會議)

2013 積體電路設計與技術國際研討會

服務機關: 國立暨南國際大學

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派赴國家: 義大利

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目次

摘要

積體電路設計與技術國際研討會（International Conference on IC Design and Technology）是全球IC設計與技術的重要論壇，以加速產品上市的時間，其中需應用到許多科學領域的技術，由設計/設備/製程技術幾大類著手，使縮短產品研發時間。而此次2013 ICICDT是在義大利的帕維亞大學（University of Pavia）舉行，會議日期從2013年05月29日至05月31日止，此次研討會是由帕維亞大學、電機電子工程師學會（Institute of Electrical and Electronics Engineers，IEEE）與Soitec公司共同舉辦。此次會議主要是針對幾項重點作為改善，像是設計/設備/製程技術的改善並衡量漏電流、耗電、雜訊等問題以及新穎材料與改變電晶體結構（例如：鰭式電晶體）和透過積體電路設計與製程技術完成新型結構（例如：PDSOI、FDSOI），希望透過這些研究能有效提升員見性能及縮短研發時間以利未來積體電路產業發展。

關鍵詞:積體電路設計、積體電路技術

壹、 目的

2013年05月25日至06月06日期間，飛往義大利的帕維亞大學（University of Pavia），參加由帕維亞大學、電機電子工程學會（Institute of Electrical and Electronics Engineers，IEEE）與Soitec公司共同舉辦的積體電路設計與技術國際研討會（International Conference on IC Design and Technology）。這次參加研討會最主要有幾個目的：發表自己最新的研究結果，並且希望能藉由參加這次研討會吸收相關知識，以便成為日後研究的方向。最後，還希望藉此次研討會多認識一些國內外的優秀學者，增加自己的溝通能力，並提升自己視野的廣度，以利於提升未來研究的高度和廣度，並期待研究能對未來台灣的積體電路產業有所貢獻。

貳、 過程

因為從台灣到帕維亞大學須長時間飛行，為了確定能如期參加研討會與調整時差，使自己保持最佳的狀態。因此，選擇提早在5月25日搭機離開台灣，途中須在羅馬轉機即可前往義大利的帕維亞大學。研討會結束後，收拾行囊準備搭機離開義大利，並在阿姆斯特丹（Amsterdam）轉機，最後在6月6日抵達台灣，結束這趟漫長的旅程。以下將簡述參加研討會之過程。

參加這次研討會最主要目的是要發表自己最新的研究結果，並希望能吸取相關新知。第一天(5月29日)參加四個會議（Trends in Power Semiconductor for Energy Efficient Applications、Silicon Photonics：An Industrial Perspective Enabling Low Cost Volume Applications、Defect-Centric Perspective of Device Reliability、From Device to Product Reliability-A Modeling Value Chain），其中最有收穫的則是頂尖學者馬尼克斯博士（Dr. Marnix Tack）的演講（題目為：Trends in Power Semiconductors for Energy Efficient Applications），恰巧演講的內容與我研究領域息息相關，主要是透過特殊的元件結構及製程技術進而達到降低功率的目的，此概念可應用在我日後研究的設計上。第二個題目主要是在探討材料分析的問題，此領域與我研究相關性並不大，不過從簡報中可得知，矽材料不僅僅使用在元件製程上，也可應用在光學領域中。三與四皆為探討可靠度的問題，前者是在討論元件可靠度的重要，因科技日新月異使得製程技術推陳出新，元件尺寸也越做越小，此現象伴隨著許多問題，其中以可靠度最值得探究，為何小尺寸元件會降低可靠度呢？主要是在於元件不斷微縮，使得以前可忽略的一些缺陷，在現今小尺寸元件中造成巨大影響；而後者主要是在研究市場量產所需的可靠度，在半導體產業中可靠度一直是發展的重要指標，如何提高可靠度大量生產是非常需要大家探究，從這兩個演講可得知，未來在做任何研究都需考慮的可靠度的問題，其中以製程缺陷及物理極限（穿隧、熱載子效應 … 等）最為重要。第二天(5月30日)這天下午三點是我上台發表論文的日子（發表論文題目為： Quantum Confinement Effect in Strained-$Si_{1-x}Ge_x$ Double-Gate Tunnel Field-Effect Transistors），發表過程尚且順利，並有專家提出問題詢

問。問題一：是否有經過實驗驗證？雖然目前尚未進行至實驗階段，但是模擬的數據與他人實驗研究的趨勢相同，這可印證我的理論是正確的，未來會利用這些數據來設計實驗，將模擬結果實體化。問題二：單閘極結構受量子束縛效應（Quantum Confinement Effect）影響會是如何？理論上如果在單閘極結構使用矽鍺材料（Strained-$Si_{1-x}Ge_x$）量子束縛效應（Quantum Confinement Effect）影響較小，原因則因量子井寬度較淺，所以影響較雙閘極結構小，此恰巧為我未來研究的內容。在這天還特別去聽穆拉里博士（Dr.Murari）的演講（題目為: Technology Push or Marketing Pull），當時看到這個題目便非常感興趣，立刻決定要參加這次的演講，主軸是在述說電子工程與市場的關係，聽完讓我體會到電子工程與市場是循環相關、環環相扣。另一個是來自日本廣島大學（Hiroshima City University）的研究報告（分享主題為: Effective Channel Length of MOSFET with Halo），內容為長通道（MOSFET）元件加上重摻雜（Halo），聽完演說讓我很有收穫，這些新穎的想法與技術，可應用在往後的研究上。在當天會議結束時，我參觀了帕維亞大學著名的伏特博物館，裡頭陳設的設備是數百年前伏特先生所使用的研究器具。其中，以真空管最令我為之驚豔，真的很難想像在數百年前以當時的時代背景，如何擁有真空的觀念以及設計出真空管的想法與技術？因為真空管內壓力極低，以當時的技術能製造出來真的是很令人讚嘆。第三天(5月31日)參加了六個會議，分別為（Emerging Technology、AMS、RF、Reliability、SoC/MPSoC/SIP、3D Integration）。會議一主要在論述未來量子元件製程技術，但目前只有理論階段並無實驗印證，其中以沒有接面的元件結構（Junction Less FET）最值得關注，因為結構簡單、製程技術容易、且元件是以傳統物理理論操作，所以未來可望實現。第二、三個會議是在探究電路問題，也讓我體認到元件應用到電路中，不單單只是元件的特性，還需考慮許多外在因素（如：電阻、電容、溫度…等問題），如此一來才能有效提高產品性能。會議四在討論可靠度問題，與前幾天不同的內容在於此次將探討更細微的基板偏壓頻率（Substrate bias-Power Frequency）的影響，此演講者提出在矽基板上進行二氧化矽/氮化矽/二氧化矽（SONOS）結構，藉由此結構改變臨界電壓（Vt）來提高元件的可靠度。會議五主要的內容偏向控制領域，與我研究內容有差異。會議六是在分享元件製程的立體（3D）技術，因為現今半導體產業主要製程技術為平面（2D），新穎的製程技術可望改善元件尺寸的微縮與降低元件耗能等問題，是未來半導體發展的重要技術。最後，在頒發表揚傑出論文後，在下午四點三十五分舉行閉幕式。當天晚上約六點時舉行餐會，經由這次餐會我結識了許多來自世界各國的優秀學者，並且相互分享研究的經驗以及成果，這對我真的是獲益良多，相信這些經驗與結果，必定能成為我日後研究很好的基礎，最後在餐會中結束為期三天的國際會議。

6月1日至6月6日主要的行程如下，因轉機，順道去參訪荷蘭的阿姆斯特丹大學（University of Amsterdam），朋友（Dr. Dong Wu and Van Bay Tran）所屬的實驗室為固態材料實驗室（Hard Condensed Matter Laboratory），實驗室內有許多新穎的製程機台，讓我大開眼界。這次參訪的主要有兩個目的，第一是期盼未來有機會能與他們合作，將我模擬的理論基礎透過實驗加以實踐出來，第二則是參加這次的研討會讓我獲益良多，在聽專家學者演講時，啟發我相關的研究靈感，可將專家學者所研究的半導體穿隧

效應（Physical Models of Band-to-Band Tunneling in Low-Bandgap Semiconductors）作更深入的探究，於是跟此實驗室彼此交流相關細節參數，這次友人分享相當多寶貴的材料參數，補足我對材料領域所缺乏的知識，對日後研究大有幫助。最後在告別的阿姆斯特丹大學後，經過長時間的搭機終於回到台灣。

參、 與會心得

我覺得參加此次研討會最大的收穫是可以結識到許多來自世界各國的朋友增加自己的溝通力，並以研究當作彼此的共通點，相互切磋討論，讓我有滿滿的收穫。透過此次研討會讓我學習到許多寶貴的研究經驗與技術，例如：如何準備好的國際會議報告；如何傾聽別人報告；如何針對報告發問好的問題；如何結識研究同伴，這些雖然在研究上不是最直接的能力，但長期來看卻是不可或缺的軟實力。最後，謝謝主辦單位帕維亞（Pavia）大學、電機電子工程師學會（IEEE）、Soitec公司讓我有機會參加此次的研討會，更感謝暨南大學能夠補助經費讓我能有這次寶貴的經驗。

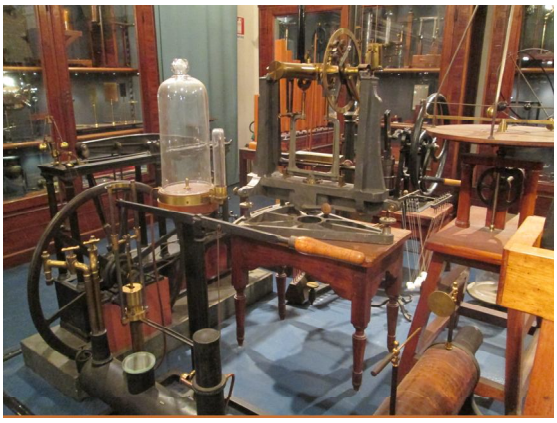
肆、 建議

1. **希望能依照不同領域的題目，能有不同的報告場地：**雖然大家研究都是IC領域，但還是可以細分為許多項目，所以在此建議主辦單位未來可以將細分的題目獨立出來，以便聽講者可更容易的選擇與自己相關或有興趣的演講題目，如此一來才能讓演講者與聽講者能有更深入的互動。

2. **期盼台灣未來也能多舉辦大型國際研討會：**台灣目前還是鮮少有大型的國際研討會，所以台灣的學生及研究人員往往都須遠赴他國才可發表研究成果，因此期待未來能爭取為大型研討會的主辦地，讓相關人員享有地利之便，讓更多人看見台灣。

附錄：會議剪影

照片一 義大利的帕維亞城市



照片四 伏特博物館（Volta Museum）

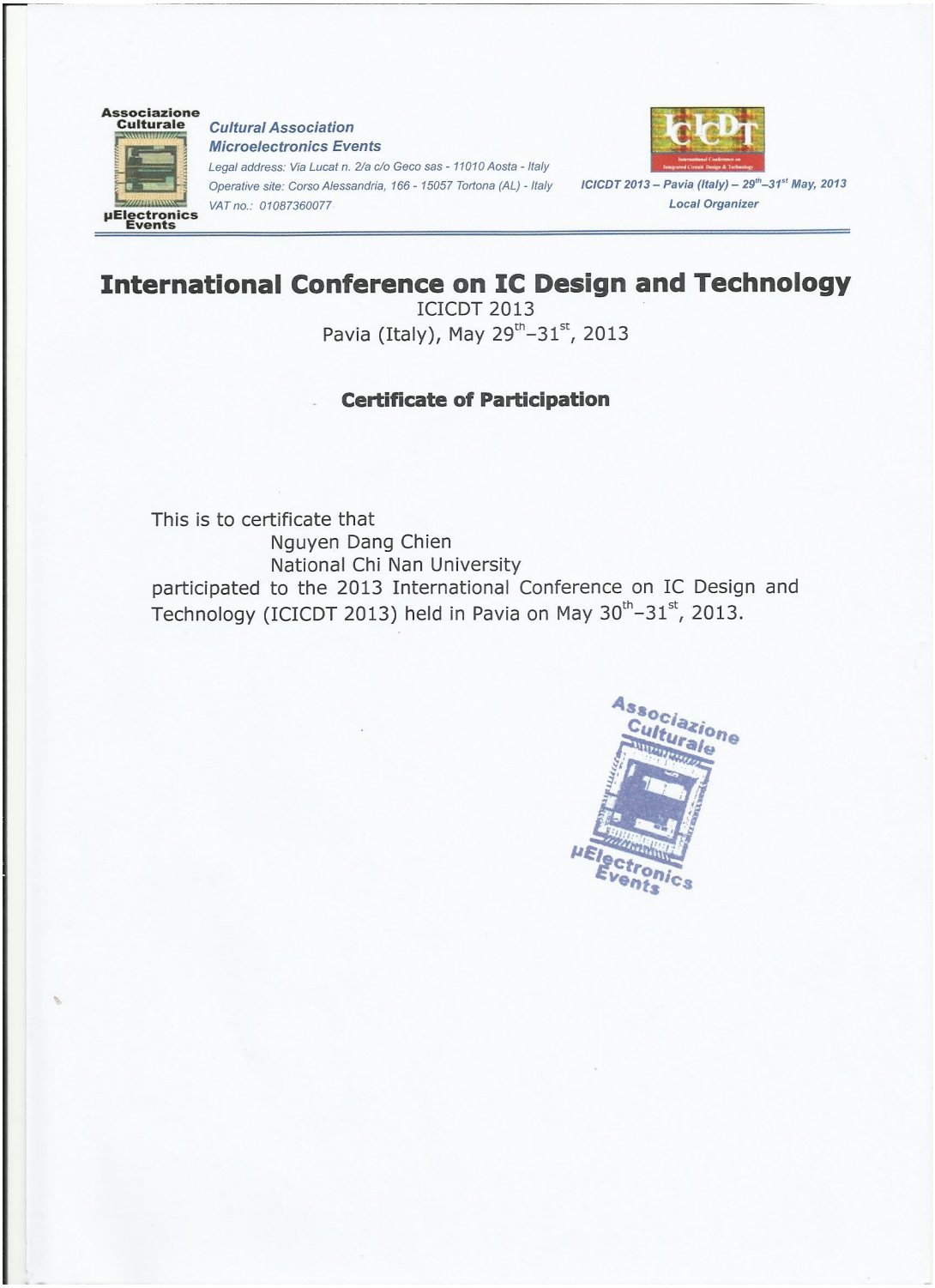
照片二 義大利的帕維亞大學
（University of Pavia）

照片五 義大利的帕維亞城市

照片三 帕維亞大學之實驗室

照片六 伏特博物館

會議參加文件



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International Conference on IC Design and Technology

ICICDT 2013

Pavia (Italy), May 29th–31st, 2013

Certificate of Participation

This is to certificate that

Nguyen Dang Chien

National Chi Nan University

participated to the 2013 International Conference on IC Design and Technology (ICICDT 2013) held in Pavia on May 30th–31st, 2013.

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Quantum Confinement Effect in Strained-$Si_{1-x}Ge_x$ Double-Gate Tunnel Field-Effect Transistors

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Abstract

The energy bandgap is a key factor to determine the tunneling current in tunnel field-effect transistors (TFETs). This paper numerically investigates the effect of quantum confinement in the double-gate TFETs by evaluating the effective energy-band bandgap of the ultra-thin strained-$Si_{1-x}Ge_x$ body. The band-offset caused by the quantum confinement effect is rapidly increased with increasing the Ge mole fraction because the body thickness must be decreased to retain the same compressive strain of $Si_{1-x}Ge_x$. A medium Ge more fraction of strained-$Si_{1-x}Ge_x$ is favorable to optimize the device performance in the strained-$Si_{1-x}Ge_x$ double-gate TFETs.

I. Introduction

Based on the tunneling mechanism, tunnel field-effect transistor (TFET) has demonstrated an excellent potential of the scalability of both the supply voltage and the physical gate length in continuing the Moore's law [1]-[4]. The quantum-mechanical calculation of band-to-band tunneling shows that the tunneling probability is strongly dependent on semiconductor bandgap [5], which has also already confirmed by experiments [6], [7]. Although a sub-60 mV/decade subthreshold swing (SS), which is a key requirement of semiconductor devices in low power integrated circuits, is achievable, Si-based TFET exhibits problematically low on-state current due to the high energy bandgap of silicon [8], [9]. Enhancing the on-state tunneling current in TFET devices becomes a considerable challenge. One of the most effective approaches to enhance the tunneling current is to decrease the tunneling barrier height by using low bandgap semiconductors. Recently, silicon-germanium alloys have been proposed in TFETs and demonstrated significant improvements in the on-state current due to its relatively small bandgaps [6], [10], [11].

It is noted that the compressive strained-$Si_{1-x}Ge_x$ on silicon substrate is preferred over the relaxed alloys for use in TFETs because of its small bandgap and low defect density [6], [7], [12], [13]. A small bandgap is helpful in boosting the tunneling current whereas a low defect density is necessary to remain a low subthreshold swing by suppressing the trap-assisted tunneling which degrades the device performance in the subthreshold region. In order to maintain the compressive strain, the $Si_{1-x}Ge_x$ layer grown on a Si-substrate is required to be thinner than its critical thickness [12], which limits the tunneling active region. For further improving the on-state tunneling current and subthreshold swing, one has used the double-gate structure as an alternative approach related to device structure of TFETs [14]. However, the use of double-gate structure causes considerable quantum confinement effect with the body thicknesses thinner than 10 nm [15]. Because the critical thicknesses of compressive strained-$Si_{1-x}Ge_x$ are extremely small at high Ge mole fractions, it is predicted that the effect of quantum confinement severely degrades the tunneling current because it makes a considerable increase in the effective bandgap.

This paper analytically calculates the effective bandgap of ultra-thin strained-$Si_{1-x}Ge_x$ body in double-gate TFETs due to the quantum confinement effect. The simulations of the TFET characteristics with and without including quantum confinement effect are compared to existing experimental data to evaluate the validity of the calculation results. The current-voltage characteristics of the devices with various Ge mole fractions are then presented to investigate the quantum confinement effect and to examine the limitation of employing low physical bandgap of strained-$Si_{1-x}Ge_x$ in double-gate TFETs.

II. Calculation of Band-Offsets

Figure 1 shows the schematic structure of a double-gate TFET with compressively strained $Si_{1-x}Ge_x$ used in the calculation of band-offsets which are defined here as

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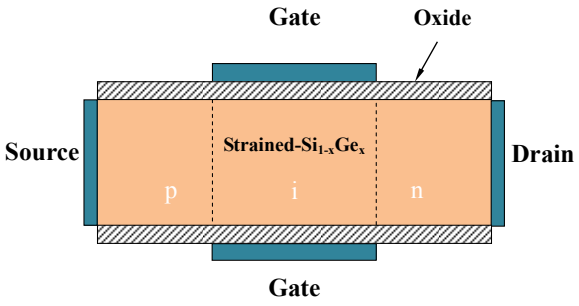

Fig. 1. Simulated structure of strained-$Si_{1-x}Ge_x$ double-gate TFETs.

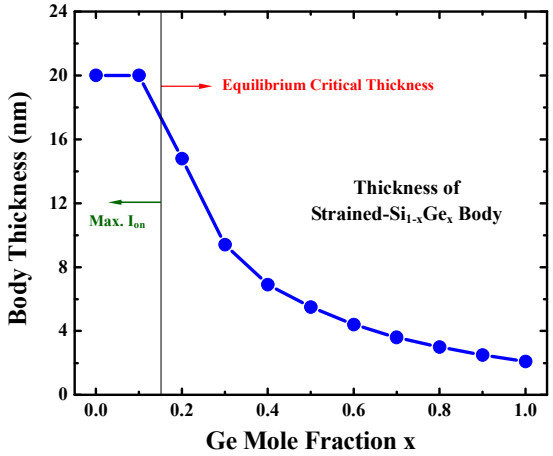

Fig. 2. Thickness of strained-$Si_{1-x}Ge_x$ body used in double-gate TFET s with various Ge mole fractions from 0 to 1.

effective changes in the conduction and valence bands under the effect of quantum confinement. Because the compressive strain is expected for Si-Ge alloys, its thickness for each Ge concentration must not be larger than the corresponding critical thickness. Fig. 2 presents the body thickness used in the calculations at various Ge mole fractions ranging from 0 to 1. At high Ge fractions, the acceptable maximum body thickness is exactly equal to the equilibrium critical thickness, whereas it is taken to be 20 nm at small Ge concentrations so that the band-to-band tunneling current is maximized [16].

Figure 3 plots the energy-band diagrams in the vertical direction to illustrate the generation of band-offsets under the quantum confinement effect. Because strained-$Si_{1-x}Ge_x$ is confined between the two oxide layers with a much higher bandgap, quantum wells for electrons and holes are formed accordingly. If the quantum wells are relatively narrow, electron and hole energies are quantized into discontinued levels considerably. Consequently, the lowest energy levels of electrons and holes in the wells will be separated from the physical conduction and valence bands, respectively, to generate

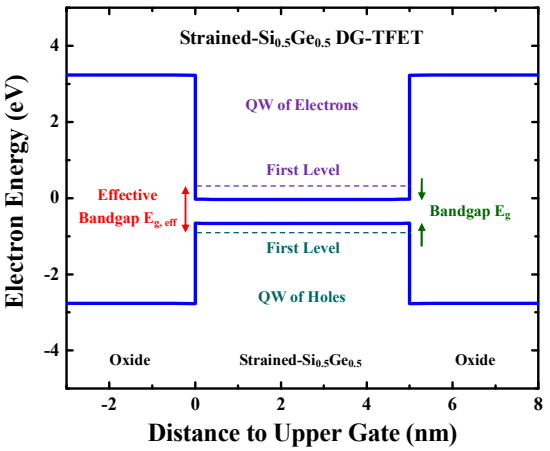

Fig. 3. Electrons and holes are confined in quantum wells in strained-$Si_{1-x}Ge_x$ double-gate TFETs (x = 0.5 for illustration).

apparent conduction and valence band-offsets.

In order to evaluate the band-offsets as well as the effective bandgap of strained-$Si_{1-x}Ge_x$, the Schrödinger equations for electrons and holes in the finite quantum wells are numerically solved to determine the quantized energy levels. Electrons on the valence-band energy levels in the channel region will tunnel to conduction-band energy levels at the drain. Because the tunneling process is extremely sensitive to the tunnel barrier height, only the first energy levels are important in determining the tunneling current. Therefore, the conduction and valence band-offsets are approximately identical to the first energy levels of electrons and holes, respectively. The effective bandgap can then be calculated as the sum of the physical bandgap and the band-offsets.

III. Results and Discussions

Since the tunneling probability exponentially changes under a variation of the energy bandgap, knowing the exact effective bandgap of semiconductor materials used in TFETs is a key issue to determine the tunneling current accurately. Fig. 4 shows the physical bandgap [17], [18], the calculated band-offset and the effective bandgap against the Ge concentration of strained-$Si_{1-x}Ge_x$ body in a double-gate TFET structure. As seen in the figure, the physical bandgap is gradually decreased with increasing Ge fraction that makes high Ge fractions favorable for TFET devices. The increasing of the Ge fraction, however, also results in a significant increase in the band-offset which degrades the tunneling current in the TFETs. Although the band-offset is negligible in the region of small Ge fractions, it becomes very significant at high Ge

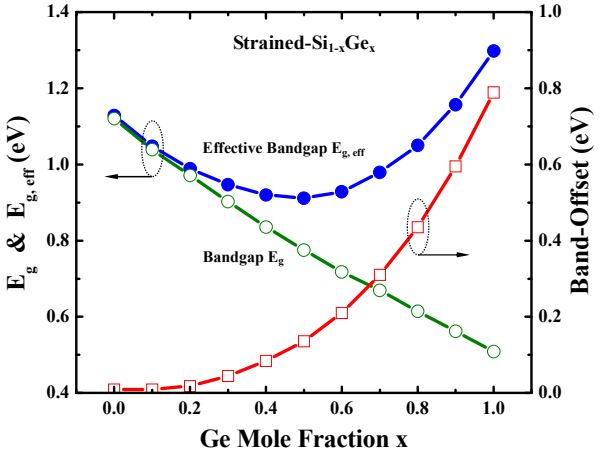

Fig. 4. Physical bandgap (E_g), calculated band-offset and effective bandgap ($E_{g,eff}$) of strained-$Si_{1-x}Ge_x$ in double-gate TFETs.

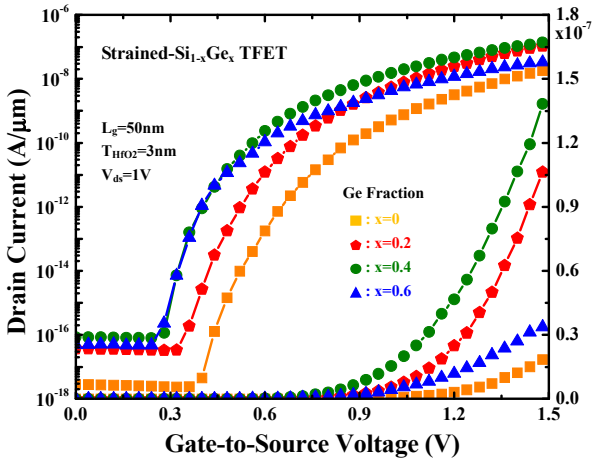

Fig. 6. Current-voltage curves of strained-$Si_{1-x}Ge_x$ double-gate TFETs with various Ge mole fractions.

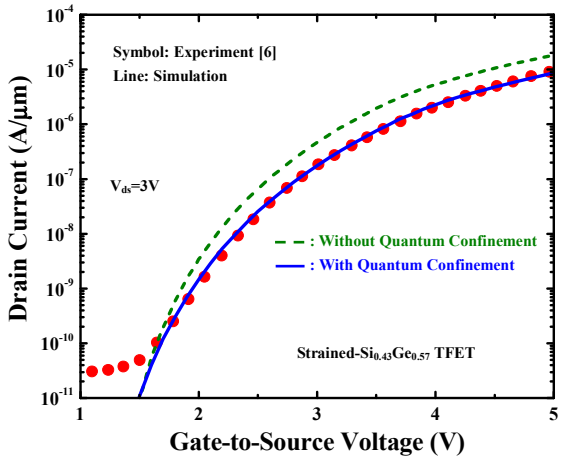

Fig. 5. Simulated current-voltage curves with and without including quantum confinement effect in comparision with experimental data of strained-$Si_{0.43}Ge_{0.57}$ TFETs [6].

fractions, even comparable to the physical bandgap. As a result of the two opposite trends when increasing the Ge concentration, the effective bandgap is first decreased down to a minimum value at a medium Ge mole fraction ($x \approx 0.5$), and is then increased quickly. Physically, it implies that the quantum confinement effect becomes dominant at high Ge fractions due to the ultra-thin body. Therefore, using strained-$Si_{1-x}Ge_x$ with extremely low or high Ge concentrations also makes a decrease in the tunneling probability due to high effective bandgaps and hence degrades the TFET performance.

The validity of the calculation of the effective bandgap is verified by comparing the simulated current-voltage curves to the measured data of strained-$Si_{1-x}Ge_x$ TFET [6]. The simulated TFET structure and device parameters are identical to those of the fabricated device in [6]. Two-dimensional device simulations [19] are performed with Kane's model of indirect band-to-band tunneling in which the band-to-band tunneling generation rate is given by [5]

$$G_{\mathrm{BTBT}} = A\frac{\xi^{5/2}}{E_g^{1/2}}\exp(-B\frac{E_g^{3/2}}{\xi}) \qquad (1)$$

where ξ is the electric field at the tunneling junction; E_g is the bandgap of semiconductors which is taken to be either the physical or effective value depending on the classical or quantum consideration adopted, respectively. The Kane's parameters A and B of strained-$Si_{1-x}Ge_x$ have been properly determined for a full range of the Ge fraction [20]. Fig. 5 shows the simulation curves with and without including the quantum confinement effect in calibration to the experimental data. Firstly, the simulated curve using the effective bandgap (the quantum confinement effect included) is remarkably lower than that of using the physical bandgap only. This implies that the tunneling current is significantly degraded by the quantum confinement effect in ultra-thin body double-gate TFETs. Furthermore, the simulation based on the effective bandgap is in very good agreement with the experimental curve, which confirms the validity of the calculation of the effective bandgaps as well as the simulation model.

In order to examine the effect of quantum confinement on the device characteristics, Fig. 6 shows the numerical current-voltage simulations of the double-gate TFETs with various Ge mole fractions of strained-$Si_{1-x}Ge_x$. At small x values, the on-current significantly increases with

increasing Ge fraction. The on-current continues increasing up to x ≈ 0.4. It is noted that the maximum on-current does not exactly occur at the Ge fraction corresponding to minimum effective bandgap (x ≈ 0.5), but at a slightly smaller value. It is because the decrease of the body thickness when increasing Ge fraction makes a decrease in the volume of tunneling region [16]. For Ge fractions higher than this value, the on-current is decreased because of high effective bandgaps and small tunneling active areas. In the view point of device performance and fabrication, therefore, it limits the exploitation of low physical bandgap of strained-$Si_{1-x}Ge_x$ in double-gate TFET devices. A medium Ge fraction should be used in double-gate TFETs for optimizing the device performance and the fabrication process.

IV. Conclusions

The quantum mechanical effect was studied by numerically solving the Schrödinger equations to determine the effective bandgaps of strained-$Si_{1-x}Ge_x$ in double-gate TFETs. Because the band offset is considerably increased with the increasing of Ge more fractions, a medium Ge fraction of the strained-$Si_{1-x}Ge_x$ is preferred to optimize the on-state tunneling current of strained-$Si_{1-x}Ge_x$ double-gate TFETs.

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