出國報告

（出國類別：其他：國際會議）

參加光學與光電 2013 學術研討會

服務單位：國立暨南國際大學 電機工程學系

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報告日期： 102 年 6 月 6 日

摘要

國際光電學工程協會(International Society for Optical Engineering, SPIE)每年於世界各地舉辦國際光電、影像、光子、光學、生物醫學、量測等相關技術學術交流會議，此國際會議上次舉辦日期為 2012 年。此會議涵蓋光子計數應用(Photon Counting Applications)、光學感測器(Optical Sensors)、量子光學與量子資訊轉換處理(Quantum Optics and Quantum Information Transfer and Processing)、高功率高能源高強度雷射技術(High-Power, High-Energy, and High-Intensity Laser Technology)、先進 X 光自由電子雷射(Advances in X-ray Free-Electron Laser Instrumentation)等相關技術領域，舉辦優秀論文發表、專家演講等項目進行，對於博士生是吸收新知與國際交流機會，透過該研討會於各領域學者進行學術交流，並將相關專業研究技術報告方式發表出去，更能展現此研討會對於此研究重視。

目錄

壹、目的

此會議為光電類別相關領域研討會，對於光電工程研究人員重要場域與國際接軌機會，更是博士生是吸收新知與國際交流機會，透過該研討會於各領域學者進行學術交流，參加國際論文發表更是語言練習機會以及上台簡報臨場展現，擴展自已國際觀視野與學術知識技術互動，可增加自我專業能力提升與競爭力比較，不同學術文化可讓學生增加不一樣思考模式，此次發表論文關於紅外線讀取電路設計討論，透過研討會方式與世界光電專家學者進行交流與會談，增加研究方法目的有所改善與建議。

貳、參加會議經過及記要

國際光電協會歐洲分會舉辦光學與光電 2013 (SPIE Optics + Optoelectronics 2013)為期 4 天研討會，地點在歐洲捷克於首都布拉格嘹亮國會飯店(Clarion Congress Hotel)，分別於 4 月 15 日至 4 月 18 日，此會議包含光子計數應用(Photon Counting Applications)、光學感測器(Optical Sensors)、量子光學與量子資訊轉換處理(Quantum Optics and Quantum Information Transfer and Processing)、高功率高能源高強度雷射技術(High-Power, High-Energy, and High-Intensity Laser Technology)、先進 X 光自由電子雷射(Advances in X-ray Free-Electron Laser Instrumentation)等等議題。透過該研討會於各領域學者進行學術交流，將相關研究作品以上台報告方式發表出去，更能展現此研討會對於此研究之重視。

4 月 13-14 日搭乘飛機中轉維也納前往歐洲捷克首都布拉格市，本研討會議於 4 月 15 日早上舉行開幕式典禮，下午開始為期四天研討會議之各項議題分組報告與海報張貼交流開始，此日排定相關議題如光電材料與光學設備方面報告，說明光學材料應用於生物感測、離子感測、細胞光量測、電子累積技術等等議題，對於本次會議涵蓋議題廣泛，本人只能就與自己研究或興趣議題進行聆聽及交流。

4 月 16 日研討會議主要在量子光學、離子累積、雷射材料累積、光元件應用、電漿離子等等，雷射材料議題上聆聽 Michal Chyla 先生演講題目”高功率，皮秒脈衝光碟雷射在祥機工程 (High-power, pico-second pulse thin-disk lasers in the Hilase project)”內容說明利用 500 毫焦耳之頻率一千赫茲及 5 毫焦耳之頻率一萬赫茲雷射實驗，將高重複率再生放大器運行在頻率一萬赫茲的脈衝下可產生能量 220 微焦耳，此放大脈衝雷射壓縮功率可提升 88%效率值，此對於雷射技術應用方面有很大幫助，如光碟機、資料儲存技術應用等。

電子累增應用議題上，由 Luca Labate 先生主講題目是”基礎小尺度的雷射電子加速器生物學和醫學生物有效性的比較研究(Small-scale laser based electron accelerators for biology and medicine: a comparative study of the biological effectiveness)”內容主要傳輸雷射光驅動電子加速器基礎之雷射之尾跡場加速(Wakefield Acceleration)過程已進入成熟的階段，此技術將被視為在醫療應用中替代使用傳統的射頻線性加速器，有效應用於放射生物醫學研究上，減少病人痛苦與治療時間。生醫感測方面一篇由 Luca Ferrari 教授主講，題目” 電化學表面等離子體共振生物感測器研究基因脫附和雜化(Electrochemical surface plasmon resonance biosensor for study of DNA desorption and hybridization)”內容包含一種結合了電化學和表面等

離子體共振技術(SPR)的感測晶片，將一個四通道之感測器的每個通道與兩個平面的電極（參考和反電極）當做輔助電極，同時監測表面等離子體共振的轉變，SPR 傳感器表面上的基因(DNA)探針可以被吸收，而不損失檢測靈敏度，可以完全檢測基因樣本，此研究對於感測器研究有不同思考面，對於實驗室生醫相關研究有不同想法。

本人在本會議文章發表於會議第三天 4 月 17 日，當日上午 10 點 10 分進行口頭報告，此分組議題主席 Josef Blazej 是捷克大學光電系教授，由於前面幾位皆為歐美人士，且報告領域關於光感測器與光學主題，故開始聆聽各位報告方式與回答技巧，這對我簡報方法學習有很大幫助，不同人員報告會是我改進的地方，且了解別人報告將是我參考與學習對象。

此場次安排受邀演講者 Andrea Cuccato 博士生主講，關於時間相關單一光子計數器，題目「緊湊 32 通道的時間解析的單光子探測系統(Compact 32-channel time-resolved single-photon detection system)」，說明如何用 32 通道方式擷取訊號，將單光子崩潰二極體用於光電倍增管，且如何完成陣列式感測電路技術說明，利用 35 奈米標準製程完成偵測設計與實驗量測，此技術用於光纖控制電路感測，對於未來高速網路應用將會有龐大產品設計與市場。再我前面一位報告演講者 Ekaterina Panina 博士生，題目「小巧的 CMOS 光子計數應用模擬讀出電路(Compact CMOS analog readout circuit for photon counting applications)」首先說明單光子雪崩二極體用於 3D 影像、電子發射斷層掃描等應用，本文重點在於如何設計陣列式感測與讀取電路設計，像素類比電路讀取設計與面積問題，關鍵於低功率、高線性度、像素均勻度等重要規格，此演講對於我研究陣列感測有不同想法，相對於單光子雪崩二極體是以單一光子產生倍率式光電流，故電路設計著重於均勻度、面積與低功率。

本次發表主題為對於歷屆紅外線讀取電路文獻可知緩衝放大器直接注入型電路與直接注入型電路主要趨勢，題目「緩衝放大器設計於雙波段紅外線感測器」(Buffer Direct Injection Readout Integrated Circuit Design for Dual Band infrared Focal Plane Array Detector)，利用 0.35um 製程完成晶片設計與實驗說明該研究技術特性，而雙波段感測器又是目前最熱門研究主題，為了配合此類型感測器特性與架構，故結合緩衝放大器直接注入型電路與直接注入型電路可增加感測器應用趨勢且降低讀取電路複雜度，實驗結果得到不同注入效率有助於不同感測器之電路應用，提升電路設計能力與系統應用種類。

報告結束後接受與會提問，由於本報告對於感測器讀取電路有相關技術提升，主席就報告內容提問”你是否有考慮感測連接讀取電路問題?”而我回答為本電路實驗為設計一像素電路想法與理念，連接

感測器有相關研究，如外接式方式、內部建立、銦凸塊(Indium bump)等，而主席又再次確認你是否有考慮銦凸塊(Indium bump)結合情形?我回答”是”，由於無人再次提問，結束本次會議文章簡報。能參加此次會議於歐美地區舉辦，讓博士生為難得學術交流經驗與磨練機會,且上台報告會能訓練自我挑戰能力與競爭力,提升不同學習視野。

最後一天上午(4 月 18 日)研討會將最後延續前天會議報告主題，有雷射於生物感測器應用、積體化光學模擬、積體化光子模型建立、雷射功率等主題，聆聽報告由 Lars Thylén 教授主講題目為“低功耗奈米光子學材料設備技術(Low-power nanophotonics: material and device technology)“內容主要說明對於光電來說其功率與空間有相當大挑戰性，鑒於光電子通信和互連構成不斷增長的需求，若減少佔用空間、功耗與成本，將可增加光頻譜寬度。光子積體化一直需要被克服與解決，此文章就是增加奈米線度光子與物質相互作用，做為光學相位調製器與相位調製器，將可產生不同頻段光譜與範圍，對於光學應用技術將有一大進展。此日另一場次由 Pierre Berini 博士主講報告為” 表面電漿子光探測器(Surface plasmon photodetectors)”此技術係為結合金屬性表面離子體之半導體檢測器，將可增強的光激發電子與提高偏振靈敏度或光譜選擇性，應用在低於矽的帶隙能量光子的輻射檢測，若能用於光通信的波長（1310 nm 和 1550 nm），針對光互連與感測應用上，適合作內部光電效應在金屬矽蕭特基接觸，對於半導體材料聚合有相當大幫助。4 月 18 日當天下午為會議閉幕式後結束本會議程。

由於往來歐洲維也納飛機班次排定問題且布拉格中轉有時間差，回臺班機需於 4 月 20 日才能由維也納搭機回臺灣，受限於時差問題於 22 日當天抵達。本次研討會亦有關於生醫感測相關領域，對於實驗室研究生醫感測器方面專業知識有極大幫助，會議演講者 Susette Germer 博士，主講以光感測應用生醫感測器，題目「聰明生物感測器應用的光子積體電路基本結構 (Basic structures of integrated photonic circuits for smart biosensor applications)」，以矽基材發光二極體產生光波導，對於生醫偵測採用不同波長檢測，應用於環境、藥物、化學鑑定能有不同感測度提升，此技術將對於實驗室研究方向進步發展。

參、會後心得

本次出國報告是學生第四次報告，在準備與臨場情況比前幾次較為有經驗，但因語言關係其簡報練習還是無法能夠很輕鬆方式報告，由於此次地點為歐洲捷克，其會場人員皆為歐美人士，是博士生難得學術交流機會，對於博士生發表會議論文於歐美地區是重要場合，此次隨行感謝指導教授孫台平院長陪同前往，讓學生感到慶幸與難得機會；感謝本次主辦單位接受學生研究論文，有機會口頭報告發表。在感測器讀取電路設計領域能以簡報方式說明自已研究方式與技術，除了發表論文外，也看到許多與自已相關研究。對我來說最大的心得就是國際學界連結的重要性，透過研討會意見交流以及與會人員相互討論，以思考自我未來研究方向、趨勢主軸。利用此機會了解本身相關研究是否在未來能結合相關技術或產品，以提升學術研究價值與質量及增加研究的競爭力。

肆、建議

對於現在博士生發表論文需要時間與專業能力，出國參加國際論文發表更是語言練習機會以及上台簡報臨場展現，透過會議交流活動能擴展自已國際觀視野與學術知識技術互動，可增加自我專業能力提升與競爭力比較，不同文化可讓學生增加不一樣思考模式，故希望有關單位能提高出國補助資源分配，尤其歐美地區研討會其費用能比鄰近國家更多資源補助，讓博士生能有口頭簡報機會與經驗表達能力。

伍、攜回資料名稱及內容

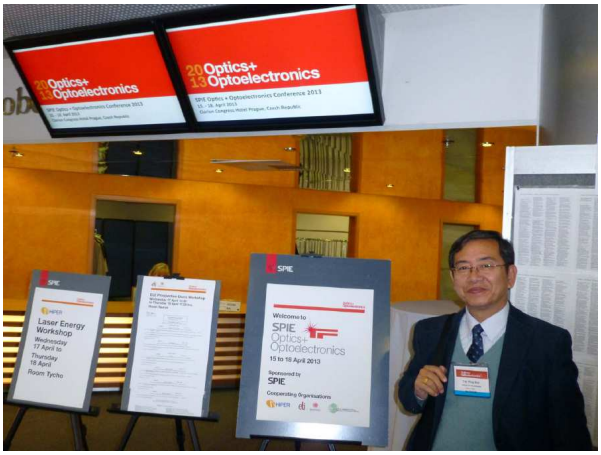
EOO 2013 會議手冊為此次會議攜帶以上資料，而全文資料需會議主辦單位會後印製再寄給與會人員，故經由已知相關論文摘要可知相關新技術研究方向與探討。另一方面藉由此會議得到許多相關領域期刊之會議徵稿，可以再將目前的研究充實及新想法實現，提升實驗室之國際觀並更加確實未來之研究方向。

陸、附錄

1.會場相關照片：

口頭報告會場

與發表會場主席合影



與指導老師於註冊會場一偶

註冊會場照片

2.本次會議口頭發表論文：

Buffer Direct Injection Readout Integrated Circuit Design for Dual Band infrared Focal Plane Array Detector

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ABSTRACT

This paper proposes dual-mode buffer direct injection (BDI) and direct injection (DI) readout circuit design. The DI readout circuit has the advantage of being a simple circuit, requiring a small layout area, and low power consumption. The internal resistance of the photodetector will affect the photocurrent injection efficiency. We used a buffer amplifier to design the BDI readout circuit since it would reduce the input impedance and raise the injection efficiency. This paper will discuss and analyze the power consumption, injection efficiency, layout area, and circuit noise. The circuit is simulated using a TSMC 0.35 um Mixed Signal 2P4M CMOS 5 V process. The dimension of the pixel area is 30×30 μm. We have designed a 10x8 array for the readout circuit of the interlaced columns. The input current ranges from 1 nA to 10 nA, when the measurement current is 10 pA to 10 nA. The integration time was varied. The circuit output swing was 2 V. The total root mean square noise voltage was 4.84 mV. The signal to noise ratio was 52 dB, and the full chip circuit power consumption was 9.94 mW.

Keywords: Buffer Direct Injection, Direct Injection, Dual Mode, Readout Circuit

1. INTRODUCTION

In recent years, the research related to dual-band infrared imaging sensors compares the aforementioned single-band sensors, which can receive signals from a larger range while improving the environmental noise tolerance to obtain an optimum signal [1, 2]. The infrared sensor material can influence the wavelength, light response, dark-current magnitude and impedance characteristics of the readout circuit device. These factors must be taken into consideration in the design of a readout circuit for an infrared sensor, along with the circuit output voltage swing,background current ,frame rate and noise.

The structure of the readout circuit for a dual-band infrared detector is comprised of two independent columns: A signal processing circuit and an output stage circuit. These columns are located on each side of the pixel circuit. If the dual-band sensors are of the same structure type, the two different wavelength sensors use two readout circuits to obtain

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the output signal simultaneously [3-5]. In infrared readout pixel circuit design, the pixel circuit layout area is limited by the sensor area. The pixel circuit design has to follow the infrared sensor specifications, while the power consumption of the pixel circuit will also have limitations. This means any design of the pixel circuit has to balance the circuit efficiency and complexity [6-8].

This paper proposes a readout circuit for dual-mode buffer direct injection (BDI) and direct injection (DI) readout circuit design. The internal resistance of the photo-detector limits the photocurrent range to affect the injection efficiency. The buffer direct injection is used for the pixel readout circuit. This is possible since the injection efficiency has improved. The buffer amplifier can reduce the input impedance to use the feedback gain of the amplifier. If the amplifier gain is greater than the feedback gain, the injection efficiency can approach 100%. The length and width of high gain amplifier occupies the pixel area. It can therefore reduce the integration capacitance to decrease the dynamic range, so the design of the readout circuit is a tradeoff between amplifier gain and pixel area. The dual band sensor is currently popular for use with infrared detectors. The designer needs to combine the advantages of DI with BDI to achieve different wavelengths for different sensor applications. This paper discusses BDI and DI; in particular, we investigate how to use a dual mode switch. To verify the feasibility and applicability of the proposed design, a 10 x 8 experimental chip was designed and implemented using a TSMC 0.35 μm 2P4M CMOS 5 V process. The circuit is separated into analog and digital sections. The analog circuit includes the pixel circuit, the column stage circuit, the bias circuit and the output stage circuit. The digital circuit includes the pixel circuit control circuit, the column select control circuit and the output select control circuit. The system architecture of the readout integrated circuit (ROIC) is shown in Fig. 1. The FSYNC signal controls the integration time of the pixels and the frame rate. The LYSNC signal controls the selection time for each row, which includes the processing time for the columns and other internal analog control circuits. The column time is controlled by the main clock, while the output time of each pixel is controlled by the rate of output from the buffer stage. The speed of the readout circuit is determined by the frame rate. The column stage includes the skimming circuit and the output buffer.

The remainder of this paper is structured as follows. The design of the infrared readout circuit is outlined, as well as the structure of the infrared readout circuit array in section 2. We also present the design of the dual-band infrared readout circuit based on the single-band infrared readout circuit. Section 3 presents the simulation results followed by the experimental results. In section 4, the conclusion and a comparison of the circuit characteristics are given.

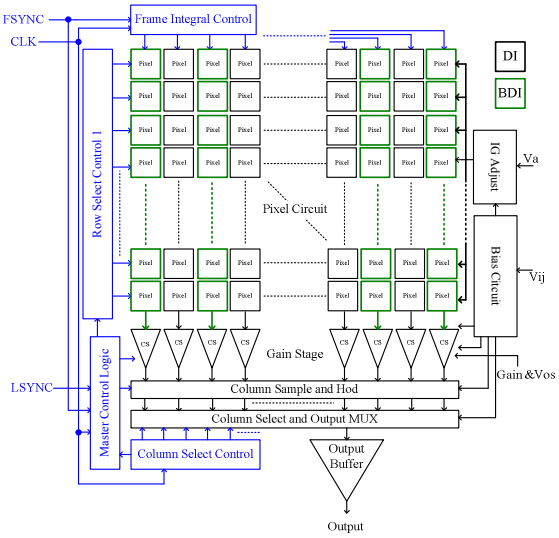

Fig. 1 Schematic showing the readout circuit of a 10 x 8 array.

2. READOUT CIRCUIT DESIGN

The system architecture of the ROIC is focused on the pixel readout circuit. There are a wide variety of technologies from the literature for use as readout circuits. The three main architectures currently used are: Buffer direct injection, capacitor trans-impedance amplification, and direct injection. For dual-band infrared sensors, the BDI combined with DI as a readout circuit is superior. A pixel readout circuit can be switched for different dual mode operation; for instance, BDI and DI, DI and DI. This section presents an illustration of the pixel and skimming circuit.

A. pixel circuit

The DI structure of the pixel readout circuit is shown in Fig. 2. The DI uses a single MOS. A detector is put on the transistor source, since the input impedance is lower. The DI readout circuit is a simple circuit with a small layout area and minimal power consumption, yet the MOS threshold voltage can be changed to affect the detector bias.

The infrared sensor is connected to the Mcp transistor source. A common connection point, Vcom, and MOS gate bias are defined, which fixes the bias voltage of the sensor. The photocurrent from the sensor is injected into the readout circuit, and the integration capacitor (C_{INT}) is integrated to the integration voltage. The integration voltage is

$$V_{INT} = \frac{I_{Ph} \cdot T_{INT}}{C_{INT}} \cdot \tag{2.1}$$

The integration voltage is passed to the sampling capacitor through the FET switch S_{sh}. The photocurrent creates the voltage across the sample and hold capacitor (C_{SH}) which will charge both C_{INT} and C_{SH}. The sampling voltage is

$$V_{SH} = \frac{C_{\text{int}}}{(C_{SH} + C_{INT})} V_{INT} + \frac{I \cdot T_2}{(C_{SH} + C_{INT})}. \tag{2.2}$$

The DI readout circuit suffers since the input impedance of Mcp is at the common gate configuration. The greater this impedance is, the worse the current efficiency becomes, and the dynamic range is hence reduced. The DI circuit architecture adds a buffer amplifier, which acts as a feedback circuit. This configuration can reduce the input resistance of the detector. The buffer amplifier gain is designed to be 40 dB. The amplifier bandwidth is 8 MHz. The BDI structure of the pixel readout circuit is shown in Fig. 3. The amplifier uses negative feedback to connect with the DI source. The amplifier is positive to bias the control detector. The layout area of the BDI is greater than the DI, to reduce the integration capacitance.

In a general detector, the equivalent model can be expressed as a parallel connection of resistance, capacitance and a current source. The impedance of the readout circuit must be very small to collect the photo current. As the detector current increases, its impedance reduces [8]. The DI source impedance is 1/gm. The injection efficiency is the performance index, which can be expressed as the ratio (η) of the input current over the detector current. The ratio (η) is

$$\frac{i_{circuit}}{i_{sensor}} = \eta = \frac{R_D}{R_D + 1/g_m}. \tag{2.3}$$

If R_D is greater than 10 times 1/gm, the injection efficiency will approach 90 %. In order to improve efficiency further to 99 %, the BDI uses a negative feedback circuit which reduces the input impedance against the amplifier gain. Equation (2.3) becomes

$$\frac{i_{circuit}}{i_{sensor}} = \eta = \frac{R_D}{R_D + \dfrac{1/g_m}{1+A}}. \tag{2.4}$$

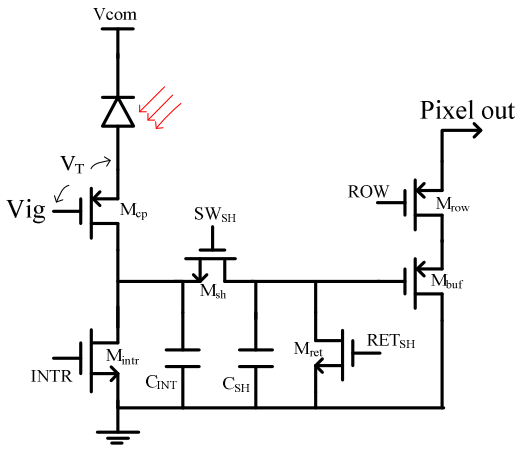

Fig. 2 DI Structure of the pixel readout circuit

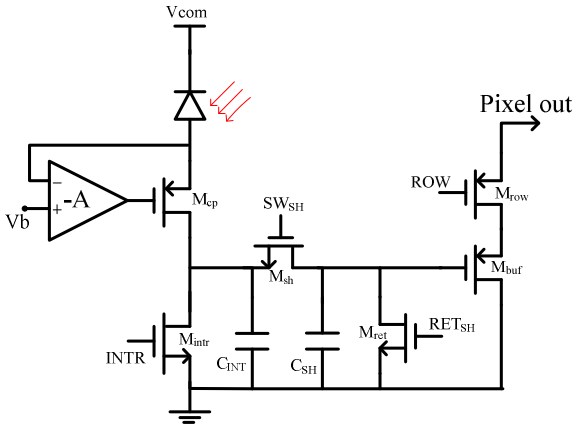

Fig. 3 BDI Structure of the pixel readout circuit

If the BDI is combined with another circuit, the DI performance results can be achieved. For example, if two band sensor detectors are used. In order to reduce the BDI layout area, the structure of the BDI uses a sharing method with a switch to achieve dual mode operation. The proposed readout circuit with the dual mode is shown in Fig. 4. The switches Φ1 and Φ2 determine the BDI and DI modes, respectively. Φ2 is the reverse of Φ1. When Φ1 is turned on and Φ2 is turned off it is in BDI mode. The voltage, Vb, can control the sensor bias directly. This BDI with improved injection efficiency and input impedance is suitable for use with long-wavelength infrared (LWIR) sensors. The BDI performed better than just DI, where Vt is changed during manufacture. In this paper, the amplifier of the BDI uses the sharing mode so that half the area of the amplifier is for the pixel. This method can reduce the pixel area and increase the integration capacitance.

If Φ1 is turned off and Φ2 is turned on the device is in the DI mode. The bias voltage, Vig can control the sensor bias through the MOS threshold voltage, Vt. If the layout and design technology is improved, Vt will not be a problem when in DI mode. The DI mode is a simple structure that only requires limited power and minimal area. For these reasons, DI is suitable for mid-wavelength IR (MWIR). The detector bias is controlled by the gate of the transistor and detector com. The gate of the transistor is important in DI mode, since the resolution of the gate bias affects the detector wavelength. In general, digital to analog converters can make use of the best bias. The half area of the amplifier can switch the pixel on/off due to the sharing mode of the amplifier of the BDI. For dual-band infrared sensors, the BDI combined with the DI as a readout circuit is superior. The switches can be selected under dual mode, so as to select BDI or DI mode.

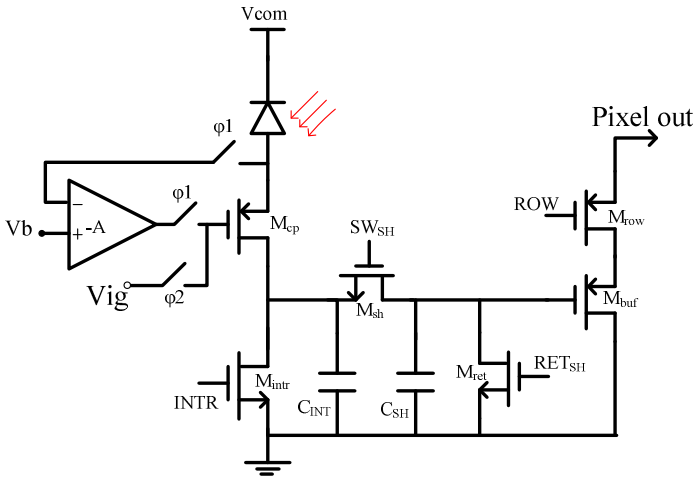

Fig. 4 The proposed readout circuit

B. Column stage

The column stage is composed of a negative feedback amplifier with switches GAIN1 and GAIN0 controlling the gain of the circuit. The gain controller can be selected under different photo currents. The combination of two switches can achieve gains of 1, 1.33, 2 and 4. In addition, the OE switches control the skimming voltage, with the VOS pin skimming the voltage [9]. The function of the skimming voltage is to avoid amplified signal saturation. The signals are amplified, and via rows selection, are delivered into the column select circuit. The aim of the circuit is to use the switches to output the signals in regular turn. The number of output points is insufficient to output the signals at the same time [9].

If we suppose the skimming voltage is used, and the output voltage steps up a voltage value, VOS, the output voltage can be expressed as

$$V_{out} = \frac{C_2}{C_1}(V_{SH} - V_{OS}) + V_{REF}. \tag{2.5}$$

3. MEASUREMENT RESULTS

The readout circuit is simulated using a TSMC 0.35 um Mixed Signal 2P4M CMOS 5 V process. The pixel layout area is 30×30 μm. The array readout circuit is 10x8 for the interlaced columns. A sensor model with a parallel connection of resistance, capacitance and current source is used. The simulation of the input current ranges from 1 pA to 10 nA. The simulated output swing is 2 V and the total power consumption is less than 9.76 mW.

Figure 5 shows the chip photograph. The I-V curve for the measurement results of a 10x8 pixel array readout circuit are shown in Fig. 6. In Fig. 6, the x-axis shows the internal current, while the y-axis is the output voltage. As the input current increases, the current injection efficiency improves. The BDI circuit architecture has superior injection efficiency, which is seen by the BDI curve approaching the calculated value. The DI structure is less efficient for high-current injection.

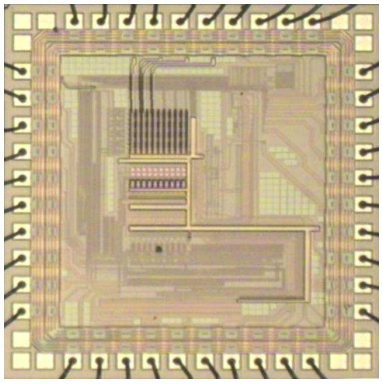

Fig. 5 Chip photograph

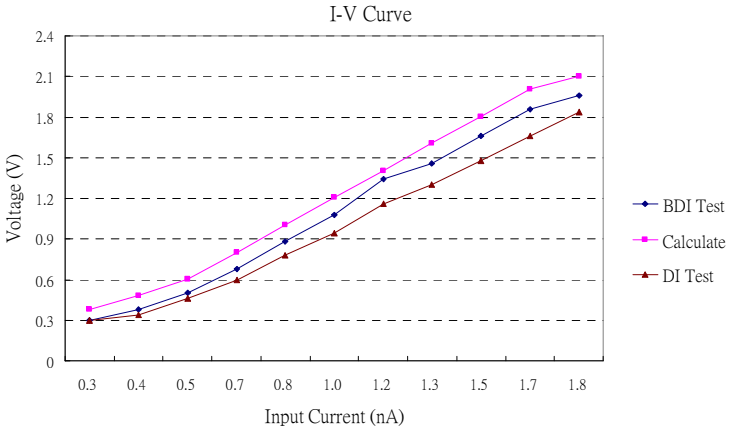

Fig. 6 The I-V curve for the measurement results

The noise can affect the performance of the readout circuit. In general, the dynamic range is an important specification, which can be expressed as the ratio of maximum signal to noise

$$DR = 20Log\frac{V_s}{V_{n,RMS}}. \tag{2.5}$$

The noise from a readout circuit is mainly caused by the capacitor noise (kTC noise). The kTC noise may be caused by the capacitance in the BDI or DI structure. The capacitor is proportional to the kTC noise. The noise in the simulation of the readout circuit is 1.07 mV. High gain on the column circuit can be used to obtain the noise signal. The total root mean square noise voltage is 4.84 mV. The dynamic range of the readout circuit is 52 dB, with a full scale voltage of 2 V.

The measured specifications of the ROIC chip are summarized in Table 1. There are many important specifications including the range of the minimum sensing current, clock rate, power consumption, frame rate, and the dynamic range.

The range of the minimum sensing current for the BDI and DI sensors under the maximum integration time is 200 pA and 10 pA, respectively. The input current is lower than the simulation, due to limitations in the measurement when using a current mirror device. The measured power consumption is also less than the simulation, due to variations in the process. The output swing is 2 V. The readout circuit noise is proportional to the kTC noise of the integration capacitor. The measured noise of the readout circuit at 300 K is 4.84 mV_{rms}. The measured dynamic range of the 10 x 8 arrays on the experimental chip is 52 dB. The integration capacitor in 30 μm x 30 μm is 0.28 pF. The frame rate and minimum integration time is 110 Hz and 20 us. The power consumption of the experimental chip is 9.94 mW, which includes the power from the output stage, the pixel circuits, the column stage, the bias circuit, and the digital circuit. If we do not calculate the output stage buffer, the total power is less than 3.5 mW. The power from each pixel follows the photo current, so the maximum power is affected by the maximum input current.

For this experimental chip, the results of the readout circuit with the dual mode under maximum integration time indicate that the BDI and DI apply to the middle wavelength and long wavelength, respectively. The long wavelength infrared detector has a lower internal resistance and larger photo current. The middle wavelength infrared detector has a higher internal resistance and lower photo current due to the sensor characteristics.

Table 1 Dual mode readout circuit array specification

Parameter	Specification	Post-Sim
Readout Pixels	10×8 pixels	10×8 pixels
Technology	TSMC 0.35um 5V 2P4M	TSMC 0.35um 5V 2P4M
Power Supply	5V	5V
Clock Rate	3.125MHz	3MHz
Total Power Without Output Buffer	< 3.5mW	< 3.24mW
Variable Gain	1, 1.3 , 2 , 4	1, 1.3 , 2 , 4
Power Dissipation	9.94mW	9.76mW
Integration Time	20us~10ms	20us~10ms
Output Swing	2V	2V
Min Input current	200pA (BDI) 10pA (DI)	100pA (BDI) 1pA (DI)
Dynamic Range	52dB	65dB
Integration Capacitance	0.28 pF	0.25 pF
MAX frame Rate	110Hz	110Hz

4. SUMMARY

In this paper, we have designed a 10x8 array for a readout circuit with interlaced columns about a dual switch mode array. The results of the BDI structure input impedance are lower than the DI structure, when each has the same input current. This results in different injection efficiencies. The dual-band sensor has different internal resistances. Direct injection is combined with buffer direct injection to create a wide range of different sensor types. Accordingly the sensor types determine the corresponding readout circuit structure. A switch control circuit was added to use BDI with DI, allowing two circuit structures in one unit cell, completing the dual switch mode array integrated readout circuit. We can choose the BDI structure to lower the internal resistance sensor, or the DI structure to separate the sensor. The ROIC achieves superior injection efficiency. The measurement current ranges from 10 pA to 10 nA. The integration time was adjusted. The circuit output swing is 2 V, system noise voltage is 4.84 mV, signal to noise ratio is 52 dB, and the full chip circuit power consumption was 9.94 mW.

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