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出國報告（出國類別：參加研討會）

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參加 International Conference on Engineering and Industries 國際研討會發表論文並參訪濟州大學

服務機關：國立高雄應用科技大學電子系

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派赴國家：韓國

出國期間：2011/11/26 ~ 2011/11/30

報告日期：2012/04/15

摘要:

本次出國主要爲參加於韓國濟州舉行之國際研討會(International Conference on Engineering and Industries)，了解在工程與各工業技術上最新發展趨勢，與國際專家交流互動，並由參加會議之Keynote/Invited Speech單元了解目前在工程與工業技術上國際上普遍關心的議題與研究發展方向，以作爲未來技術研究時可參考的主題，此外，也在該研討會發表論文，論文主題爲「Novel High-CMRR DVCC-based Instrumentation Amplifier」，並觀摩會議中其他技術研究論文，了解目前電子工業技術的發展現況，另外，並在會議開會前參訪濟州國立大學，對該大學的教學環境有基本的認識。

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本文:

一、 目的:

本次出國主要爲參加於韓國濟州舉行之第二屆工程與工業國際研討會(International Conference on Engineering and Industries)，了解在工程與各工業技術上最新的發展趨勢，並與國際技術專家交流互動，本研討會爲 IEEE Circuits and Systems Chapter 所贊助之國際性重要研討會之一。

本年度的工程與工業國際研討會與另三個國際研討會一起舉辦，即6th International Conference on Computer Sciences and Convergence Information Technology、7th International Conference on Information Processing and Management與2nd International Conference on Advancements in Computing Technology，這些會議之會議主題領域相關，涵蓋電腦科學、資訊處理與管理、運算技術等。另外，並在會議開會前參訪濟州國立大學，對該大學的教學環境有基本的認識。

二、 過程

本次出國期間爲2011/11/26 ~ 2011/11/30，主要爲在國際研討會上發表論文，在會議開議前抽空先參訪濟州國立大學，行程如下:

日期	行程
100/11/26	啟程到桃園機場搭機赴韓國濟州
100/11/27	參訪濟州大學
100/11/28	會議報告事項
100/11/29	會議報告事項
100/11/30	會議報告事項 回程返台(韓國濟州->桃園機場→高雄)

濟州國立大學離濟州市約一小時車程，本次參觀其電子系，電子系辦門口並無英文標示，校園內英文標示也很少。然而卻是韓國重要的國立大學之一。濟州國立大學位於韓半島西南端，是連接其他國家的要塞之地，又具有得天獨厚的自然景色，是世界著名觀光和修養勝地。濟州大學建立於1952年，濟州大學堅持求實，不斷創新，積極探索獨特而新穎的教學發展模式，受到國內外的關注。

濟州國立大學的網址爲http://www.jejunu.ac.kr/，校訓是真理(Truth)、正義(Justice)、創造(Creation)，其夥伴學校包括很多國家，台灣亦有七所大學機構與之簽署夥伴學校，該校也有交換學生與雙學位修讀制度，目前其研究所招收國外學生之科院別如下表:

程度	學院	部門
碩士學位	人文學科 &社會科學	韓國語言和文學、日語和 文學、中國語言和文學、英文和文學， 德國研究、歷史、社會學、哲學、公共事務管理、 政治學&外交、新聞事業&公共關係， 經濟，國際貿易，工商管理，會計， 管理信息系統，旅遊業管理，旅遊業發展， 農業經濟學
	自然科學	不傷環境的 農業、園藝、漁場科學、地球和海洋科學、生物、化學、食品科學&營養、數學、 計算機科學&統計、家庭管理、衣物&紡織品、護理、生物工藝學、海洋生物科學、應用的生活工程學、生物醫學&新的藥物發展、動物生物工藝學
	科學和工程學	應用的 能源系統學部 -主修物理 -主修機械工程

		-主修能量和化學工程 -主修電機工程 -主修電子工程學
	工程學	食品科學&工程學、電信工程學、 計算機工程、建築學、環境工程學、民用 &海洋工學、海洋信息&系統工程，機電工程學
	藝術和體育	體育，藝術，音樂
	醫學	獸醫，醫學
	跨學科計畫	生物醫學工程，韓國研究，海洋氣象學，財政信息
博士學位	人文學科 &社會科學	韓國 語言&文學、英文&文學， 公共事務管理、工商管理、農業經濟學、旅遊業 管理、中國語言&文學、會計、社會學、 管理信息系統、政治學、國際貿易、旅遊業發展、歷史、日語&文學、新聞事業& 公共關係，教育，哲學，法律 語言教育學部 - 主修韓國語言教育 -主修英文教育 -主修基本英文教育 社會科學教育學部 -主修社會學教育 -主修地理教育 -主修基本社會學教育 道德倫理教育學部 -主修倫理教育 -主修基本道德教育

	自然科學	友善環境農業， 園藝學， 生物工藝學， 漁業科學， 海海洋生物科學， 地球和海洋科學， 生物學， 化學， 數學， 計算機科學和統計，食品科學和營養，家庭管理，衣服和紡織品，應用生命科學，生物醫學和新藥發展，動物生物工藝學 科學教育學部 -主修物理教育 -主修生物教育 -主修計算機教育 -主修基本科學教育 -主修基本實用藝術教育
	科學和工程學	應用能源系統學部 -主修物理學 -主修機械工程 -主修能源和化學工程 -主修電機工程 -主修電子工程
	工程學	食品科學&工程學、電信工程學、 計算機工程、環境工程學、民用&海洋工學、 海洋信息&系統工程、 機電工程學
	藝術和體育	體育
	醫學	獸醫，醫學
	跨學科計畫	生物醫學工程，韓國研究，海洋氣象學
碩博士	人文和社會科	英語和文學， 公共行政，工商管理，農業經濟學，旅遊

一貫學位	學	管理，漢語和文學，會計學，管理資訊系統，旅遊發展，歷史
	自然科學	友善環境農業， 園藝學， 生物工藝學， 漁業科學， 海海洋生物科學， 地球和海洋科學， 生物學， 化學， 數學， 計算機科學和統計，食品科學和營養，家庭管理，衣服和紡織品，應用生命科學，生物醫學和新藥發展，動物生物工藝學
	科學和工程	應用能源系統學部 -主修物理學 -主修機械工程 -主修能源和化學工程 -主修電機工程 -主修電子工程
	工程	食品科學和工程，電信工程，計算機工程，環境工程，市民和海洋工程，海洋訊息和系統工程。 計算機控制精密機械設計與製造學工程
	美術和體育	體育
	藥	獸醫學，醫學
	跨學科計畫	生物醫學工程，朝鮮語研究，海上氣象學

本次參訪濟州國立大學電子系，該系師資包括六位教授與一位助理教授，專長領域包括:電腦網路、半導體元件與製程、印刷電子與光信號處理、儀表與控制、電阻抗斷層攝影、光電子、電腦輔助電路設計、神經網路、通訊與雷達系統信號處理等，該系在1993年與1999年分別設立碩士與博士班，該系教授之主要課程爲: circuit theory, communication theory, electronic circuit, applied electronic circuit, digital engineering, physical electronics, semi

conductor engineering, control engineering, sensor engineering, multimedia engineering, optoelectronics, integrated circuit manufacturing, digital system, embedded system, ubiquitous system, digital signal process, microprocessor, design of computer use, Location Based Service, neural circuits network, telematics, home network, IT design, IT practice等等，幾乎涵蓋電子工程的所有重要領域。

三、 心得

濟州國立大學除包括如上述非常多的專業領域發展，在海外也有很多招生宣傳據點，校園環境優美也是其特色，每年春季吸引不少賞櫻人潮，但其校園國際化環境並不佳，例如路線大樓指引僅有韓文標示，電子等系所也不見英文標示。

本次工程與工業國際研討會之Keynote/Invited Speech單元，第一場是韓國Dr. Jung Uck Seo演講「Science and Engineering for Sustainable World」，他獲有博士學位與經濟榮譽博士學位與工程榮譽博士學位，曾任韓國科學與科技部長，也是IEEE理事會成員之一，其講述重點在環境與科學技術的平衡發展，即現在所常提到的綠色電子。另一場是日本Prof. Yen-Wei Chen演講「Digital Atlases of Human Anatomy and Their Applications to Computer Assisted Diagnosis」，Prof. Yen-Wei Chen為日本大阪大學博士，現在為Ritsumeikan University資訊與工程學院副院長，經歷英國牛津大學與美國賓州州立大學訪問教授，講述重點在醫用電子資訊方面，即應用人體解剖影像技術作輔助診斷應用。由以上演講主題可知，工程與工業技術上國際上普遍關心的議題與研究發展方向在環保節能電子設計與生醫電子，這兩個主流發展方向關係著人類生活品質與環境的維護，近年來環境的急遽變遷，許多的天災不斷發生，例如乾旱、雪崩、地震、海嘯、颶風、疾病、洪水、熱浪、暴雨大浪等接踵而來，希望在科技工業發展上，能提升防災功效，並在科技發展與環境維

護上取得平衡，將維持人類與其他生命物種生存永續視爲重要議題。

由本會議中所發表之論文，可觀察到在工程與各工業技術上最新發展趨勢包括的主題有:航空資料查詢最佳化、地鐵監控控制系統、高效能家庭網路、動作辨識特徵選擇技術、強健控制器之滑動模擬、三軸橡膠測試機研發、強健設計最佳化在反轉問題與最小平方法之比較、使用太陽能板之混合開關電源供應、心電圖R-peak之快速偵測演算法、低雜訊儀表放大器設計等。包含的主題有網路通訊、儀器控制、影像處理、生醫電子設計與訊號處理等。

個人則於本會議發表論文論文主題爲「Novel High-CMRR DVCC-based Instrumentation Amplifier」，屬於高性能電子電路研究新知的發表。其全文內容如附件。

四、 建議事項

濟州國立大學在韓國算是10名以內的知名大學，也招收不少國際學生，但以中國留學生居多，其校內英文環境並不好，路線大樓指引僅有韓文標示，電子等系所也不見英文標示。學生聽到講英文的人反應都很緊張，然而校園環境優美面積大是其優點，搭配濟州觀光旅遊人力需求也有相關系所(如旅遊業管理，旅遊業發展系所)之設立，基本上觀光業算是低污染高價值產業，其學生英文能力不太好，即使參與國際研討會之工程師英文能力也不佳，但其守法與敬業精神倒是不輸台灣學生，這從街道建築物的整齊，市區鳴喇叭聲音不多可窺知一二。

附錄

1．發表論文內容

2．參加研討會與參訪濟州大學相片

Novel High-CMRR DVCC-based Instrumentation Amplifier

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***Abstract*- A novel instrumentation amplifier (IA) is presented in this article. The proposed IA possesses improved performance in comparison with the common current conveyor-based IAs. It consists of two differential voltage current conveyors (DVCCs) and two resistors. The non-ideal effects of the active devices are discussed. Performances of the proposed circuit are confirmed through HSPICE simulation. The simulated results show that the common-mode rejection ratio (CMRR) of the proposed CMIA is 102 dB up to 6.13 MHz in TSMC 0.18μm 1P6M CMOS technology with 1.8V DC power supply.**

I. INTRODUCTION

An instrumentation amplifier (IA) is an important block in many areas such as data acquisition, medical instrumentation and signal processing applications. It requires wide bandwidth and high CMRR to suppress the unwanted common-mode signals [1-2]. For voltage-mode IA, the three-operational amplifier-based topology is the most popular one, as shown in Fig. 1. However, this structure has some drawbacks because its CMRR is limited by the mismatch of resistor components and the operational bandwidth of IA is suppressed by the constant gain bandwidth product of the operational amplifiers [3-5]. To overcome these drawbacks, much attention has been paid to the design of current-mode instrumentation amplifier (CMIA) due to featuring very high bandwidth and a CMRR insensitive to resistor mismatching which is the big problem of the voltage-mode IA. Fig. 2 shows a high-CMRR IA design without the need of any resistor matching condition. It also enables high differential gain without the drastic bandwidth reduction inevitable with traditional operational amplifier circuits [6-7].

Although the CMIA in [6] does not need good resistor matching, its CMRR is not good enough for practical application. An improved CMIA with current subtraction mechanism using the operational amplifier was developed in [8] and is redrawn in Fig. 3. The CMRR improvement of this circuit is due to the output current of the second conveyor subtracting from the output current of the first conveyor [4]. But the use of operational amplifier limits the CMRR of this IA. A further improved version of CMIA is reported in [9] and shown in Fig. 4, this IA makes use of the current feedback technique to achieve high-performance characteristic. In this paper, a high-CMRR DVCCs-based IA using current feedback technique is proposed. HSPICE circuit simulator is used to verify the performance of the proposed IA. Three popular CCII-based IAs are constructed for performance comparison.

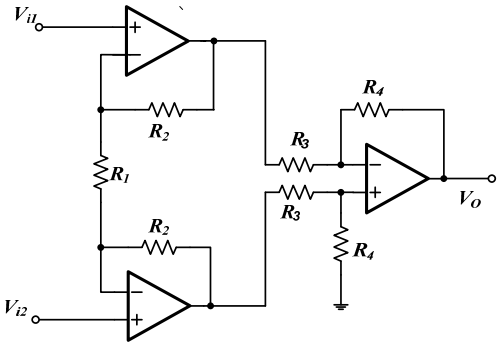

Fig. 1 Three-operational amplifier-based IA

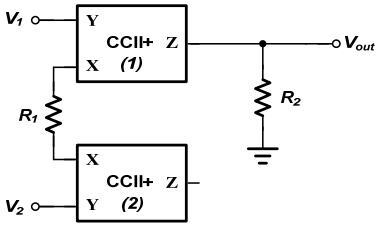

Fig. 2 High-CMRR IA

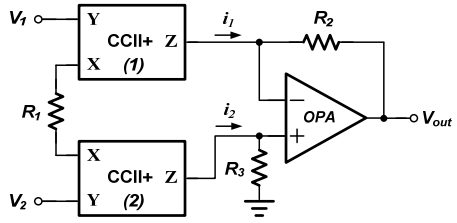

Fig. 3 An improved high-CMRR CMIA

II. CIRCUIT DESCRIPTION

The CMIA in [9] comprises two plus-type second generation current conveyors (CCII+s) and two resistors, as shown in Fig. 4. The CCII+ is a three-terminal active device with terminal characteristics described by

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & \beta & 0 \\ 0 & 0 & 0 \\ \alpha & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \end{bmatrix} \quad (1)$$

In (1), non-ideal current gain $\alpha = 1-\varepsilon_i$ and non-ideal voltage gain $\beta = 1-\varepsilon_v$ are ideally equal to unity. In addition, $|\varepsilon_i| << 1$ and $|\varepsilon_v| << 1$ are respectively called current and voltage

tracking errors. Considering the non-ideal transfer gains of the CCII+, the output voltage can be given by

$$V_{out} = \alpha_1(1+\alpha_2)(\beta_1 V_1 - \beta_2 V_2)\frac{R_2}{R_1} \quad (2)$$

For the differential inputs $V_1 = V_d/2$ and $V_2 = -V_d/2$, the corresponding differential-mode gain A_{dm} can be expressed as

$$A_{dm} = \frac{V_{out}}{V_d} = \frac{\alpha_1(1+\alpha_2)(\beta_1+\beta_2)}{2}\frac{R_2}{R_1} \quad (3)$$

For the common-mode input $V_1 = V_2 = V_{cm}$, the corresponding common-mode gain A_{cm} can be expressed as

$$A_{cm} = \frac{V_{out}}{V_{cm}} = \alpha_1(1+\alpha_2)(\beta_1-\beta_2)\frac{R_2}{R_1} \quad (4)$$

From equations (3) and (4), the CMRR can be expressed by

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{\beta_1+\beta_2}{2(\beta_1-\beta_2)}\right| = \left|\frac{2-\varepsilon_{V1}-\varepsilon_{V2}}{2(\varepsilon_{V2}-\varepsilon_{V1})}\right| \quad (5)$$

From (5), it is found that the CMRR is independent of current gains of both CCIIs.

Even the CCII has been proved to be a versatile building block, which still has a disadvantage that only one of the input terminals has high input impedance. The DVCC is an extended version of CCII. It was first proposed in 1997 [10]. The DVCC provides two high-impedance terminals to handle differential-input voltage signals. The new proposed CMIA topology consists of two DVCCs and two resistors, as shown in Fig. 5. The DVCC+ is a four-port building block with terminal characteristics described by

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \quad (6)$$

where $\alpha = 1 - \varepsilon_i$ and $\beta_j = 1 - \varepsilon_{vj}$ for j =1, 2 are non-ideal current gain and non-ideal voltage gain, respectively. Here ε_i and ε_{vj} ($|\varepsilon_i|$, $|\varepsilon_{vj}| << 1$) respectively represent current and voltage tracking errors of the DVCC+. Denoting β_{1i} , β_{2i} and α_i (i =1, 2) as mentioned parameters associated with the ith DVCC+ in Fig. 5. Reanalyzing the IA circuit in Fig. 5, the output function can be given by

$$V_{out} = \alpha_1(1+\alpha_2)[(\beta_{12}+\beta_{21})V_2 - (\beta_{22}+\beta_{11}V_1)]\frac{R_2}{R_1} \quad (7)$$

For the differential inputs $V_1 = V_d/2$ and $V_2 = -V_d/2$, the corresponding differential-mode gain A_{dm} can be expressed as

$$A_{dm} = \frac{V_{out}}{V_d} = \frac{-\alpha_1(1+\alpha_2)(\beta_{12}+\beta_{21}+\beta_{11}+\beta_{22})}{2}\frac{R_2}{R_1} \quad (8)$$

For the common-mode input $V_1 = V_2 = V_{cm}$, the corresponding common- mode gain A_{cm} can be expressed as

$$A_{cm} = \frac{V_{out}}{V_{cm}} = -\alpha_1(1+\alpha_2)(\beta_{12}+\beta_{21}-\beta_{22}-\beta_{11})\frac{R_2}{R_1} \quad (9)$$

From equations (8) and (9), the CMRR can be expressed by

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{\beta_{12}+\beta_{21}+\beta_{22}+\beta_{11}}{2[(\beta_{22}-\beta_{21})-(\beta_{12}-\beta_{11})]}\right| \quad (10)$$

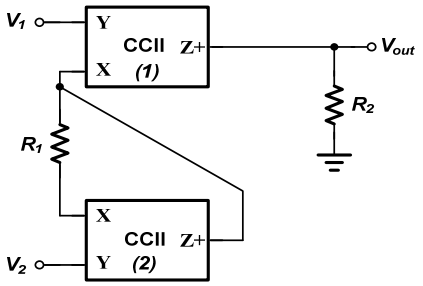

Fig. 4 High-CMRR CCII-based IA

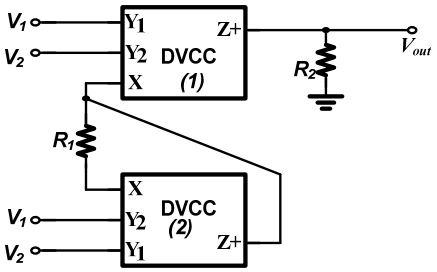

Fig. 5 The proposed high-CMRR DVCC-based IA

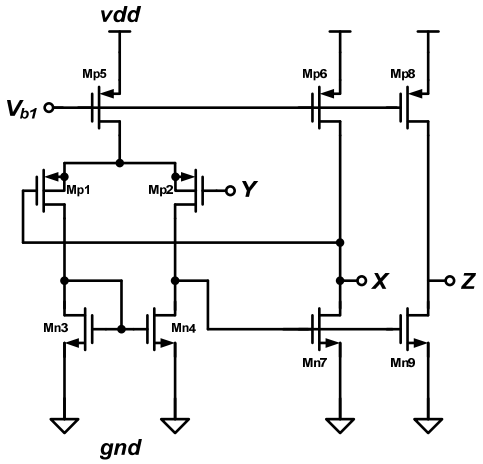

Fig. 6 CMOS realization of the CCII

From (10), it is found that the CMRR is independent of current gains of both DVCC+s in Fig. 5. Also, by observing the denominators of (5) and (10), it can be found that the CMRR in (10) will be increased if the non-ideal voltage gains of the DVCCs have the same variation trends.

III. SIMULATION RESULTS

To verify the potentialities of the proposed DVCC-based IA, the CMIAs described in Figs. 2-5 are simulated using HSPICE in TSMC 0.18um CMOS technology with 1.8V DC power supply. The CMOS implementation of the CCII in [11-13] is used to construct the CCII-based CMIAs mentioned above. The scheme of the CCII is shown in Fig. 6. The DVCC structure is based on this CCII with the adding of one additional differential pair, as shown in Fig. 7 [10]. For the

TABLE I
Performance list of the IA in Figs. 2-5

Simulated Parameter	**Fig. 2**	**Fig. 3**	**Fig. 4**	**Fig. 5**
$\mathbf{f_{-3dB}}$(MHz)	4.67	4.58	5.21	6.13
$\mathbf{A_{dm}}$ (dB)	12.1	12.1	12.1	12.1
$\mathbf{A_{cm}}$ (dB)	-16.7	-35.9	-34.3	-89.9
CMRR(dB)	28.8	48	46.4	102

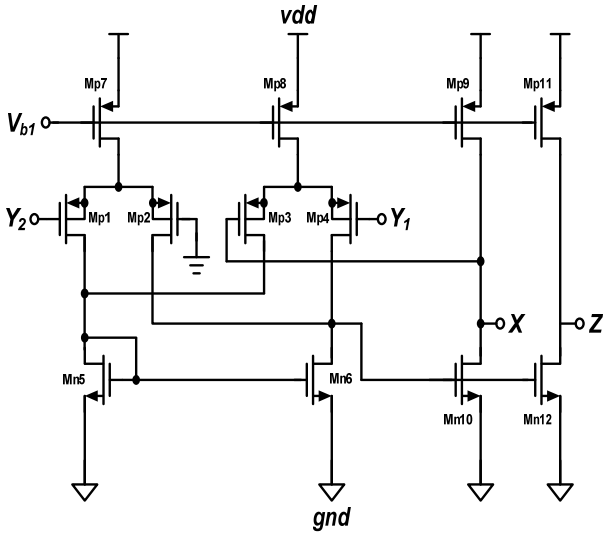

Fig. 7 CMOS realization of the DVCC

performance comparison of the IAs in Figs. 2-5, the differential-mode gain (A_{dm}) of 12.1 dB is used for all IAs. The simulated result of each IA in Figs. 2-5 is given in Table 1. It shows that the common-mode gain of the proposed IA in Fig. 5 has been decreased evidently. The simulated result reveals the feasibility of the proposed circuit.

IV. CONCLUSION

In this paper, a new DVCC-based CMIA is presented. The proposed CMIA has improved CMRR performance in comparison with three CCII-based IAs in the literature. The workability is verified by HSPICE simulation.

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