行政院及所屬各機關出國報告
（出國類別：考察）

CDMA 歐洲訪廠評估報告

服務機關：中山科學研究院
出國人職稱：副所長　研究員　副研究員
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出國地區：歐洲
出國期間：89 年 12 月 2 日至 89 年 12 月 10 日
報告日期：90 年 1 月 9 日

一、 出國目的及緣由

目的：執行經濟部科專寬頻無線通訊系統發展計畫之技術引進訪廠評估及規格擬定。

緣由：本院三所執行經濟部委託之科專「寬頻無線通訊系統(WB-CDMA/WLL)設計專案」技術移轉工作，九十年度技術引進項目為基頻信號處理及通訊協定，針對未來技引合作對象，必須瞭解其技術能力、經驗及相關智慧財產權而進行訪問廠商及研究機構，並制定 RFP(Request for Proposal)技引規格。

二、 公差心得

1. 無線科專之技術層次不論用戶台、基地台之 RF、IF 及 Base band 或者通訊協定，各公司均積極發展自己的 IP，並不輕易技轉給他人，以明年度的技引工作，在有限經費下如何能獲得最需要之技術，是件很艱鉅的事，以 Base band 為例，必須要有自己的實力，才可能在技引過程中雙贏。因此技術團隊實力之加強為當務之急，Protocol 部份沒有二、三百人研究實在無法切入，目前做法以本院所需的為第一考慮，如 RLC、RRC 及 MAC，再配合資策會電通所已有之 Protocol 經驗來共同發展。

2. 本院以往研發工作，多為重視硬體而不太重視軟體，但在 3GPP 之 WB-CDMA / WLL 軟體所做之比重遠大於硬體，尤其到 RNC，CN 等更上層之工作，若沒有完整之規畫及研究方式，則無線通訊之發展永遠受制於人，淪到代工。國內推動無線通訊已有五、六年，由於工作分散，目標不確定，缺少大師級人物領導，執行計畫經常換手，造成與歐美甚至韓

國及大陸之技術差矩越來越大，本院執行無線科專僅為此計畫中之一環，能做好計畫內之目標已屬不易，但又往往遭遇內憂外患，幾致停擺，所幸有一批人忍辱負重，願意繼續朝目標努力，也算是異數。

三、 效益分析

由於 WB-CDMA 之技術層次及複雜度很高，在執行技術引進時所提出之規格書內容牽涉很廣，在制定時必須參考各公司之實力及經驗及本科專計畫之需求，因此本次參訪格外重要。在與 Sirius Communication Co. 討論研究後完成下列技引之規畫書及相資料，對未來技引案之規畫，執行有極大之勵益，各項資料如下：

1. WB-CDMA/WLL 基頻信號處理技術引進規格需求書一份參考附件一)
2. WB-CDMA/WLL 通訊協定技術引進規格需求書一份參考附件二)
3. WB-CDMA 通訊協定中 RNC 之研究分析報告(Tality 公司提供比利時某大電訊廠商之研究規劃書)(參考附件三)

四、 國外工作日程表

12/2-12/3：起啟自桃園至比利時布魯塞爾

12/4

本日主要是與 Sirius Communication (SC)公司討論有關技術引進之細節問題，其中包括(1)規格制定(2)技引項目(3) Schedule，分別說明如下：

(1) 本院所執行之 WB-CDMA/WLL 符合 3GPP Release 99 之 Air Interface 雖已提出規格，但由於本項技引工作為基頻信

號處理 (Base band)，故有部份必須詳細律定，其中包括 Base band 所使用之 Algorithm，與 Controller 之介面，BER 之標準等等，因此花了相當多時間針對來回 E-mail 及 FAX 中 50 多項疑問逐一澄清，預計 12 月 15 日前定出技引規格辦理購案準備工作(此為公開招標，故 Spec 必須詳細)。SC 公司並提出 FPGA 版本之架構，必須用戶台及基地台均能使用 (參考附件 1) 。其中仍有諸多待商榷之處，如：如何與本院設計之 IF/RF 搭配。本計畫所選用之 ARM7 Processor 之執行能力是否可以 Cover Base band 之控制，基地台之 RACH 數目是否可以擴大等等，將與二十組及八組討論再做最後版本。

(2) 目前技引項目為：用戶台包含 FPGA Based 之 Base band 信號處理(Inner Receiver) ARM 7 之 Control 介面及 Source code 各 Algorithm 之 Simulation 方法及結果等詳細之文件。基地台包含二片 FPGA 之基頻信號處理(RACH 及其他)，ARM 7 之控制介面及 Firmware Source code 等。

(3) 目前規畫時程是 90 年 1 月提出公開招標購案(由國防部核批)，明年 2 月科專預算核下來則開標作業，4 月份開始技引，10 月份 Proto type demo，12 月之 64K bps demo 則可用此技引之結果。

12/5

本日主要參觀 Cadence (Tality)之愛丁堡公司，Tality 在愛丁堡有一非常完整之 Design center，其中包括 3G Infrastructure， SOC 及 Protocol 小組，其中 Protocol 小組目前正執行歐洲等大公司之 3GPP 通訊協定中之 RNC 設計，Dr. Moore 詳細說明此 RNC 之設計 Procedure(無法提供紙本給我

們)，其中包含了不少我們想技引之技術，此點將會與電通所討論，光是 RNC 之設計，Tality 公司有 18 位有經驗工程師花一年半時間才完成 Proto type 之版本。因此對我們給 Tality 所做之簡報，他們均認為要在未來 3 年內完成所有 protocol 之設計，實在困難。因為 3GPP 之通訊協定一直沒完全定案，Tality 公司是邊做邊修，而且 Tality 為協定制定之成員，可以很容易拿到第一手之資料，本院因不能參加此種組織，故在執行工作時往往落人後，只有靠技術引進來縮短研發時程。經我們虛心求教，總算拿到簡化版之 RNC 架構，將提供給二十組參考(參考附件 2)。

12/6

本日主要是與 Tality 公司 Cambridge 部門討論有關目前技引之計畫及明年可能合作之通訊協定合作案，內容包括：

(1) 本年度之技引，原則上已完成 WPI 之報告(RRC 及 RLC)。並於 12 月中旬交給資策會，Tality 工程人員亦 demo 此項工作之 Simulation 結果(SDL 版本)，基本上 Cambridge / Tality RRC 及 RLC 均有資深工程師參與設計，結果可以用在明年 12 月份之 Demo。

(2) 由於通訊協定太廣，雖然明年有一億五千萬元之計劃外之技引(由電通所、中科院及資策會三方面共同引進)，但要完全 cover 3GPP 之 Protocol 仍不可能，故我們要求 Tality 給一個完整之 Proposal，包含每一 Module 之時程及價格，再由我們之實際需要，demo 時程來決定採取何種技引及內容(參考附件四)， Tality 公司同意，並將於 12 月底前提出 Proposal，目前我們要求仍以明年 12 月 demo 之通訊協定為優先考慮(包含完整之 RRL，RRC MAC 之 source

code，portion 在我們的平台上，RRM 之 SDL 及與 PDCP 之介面設計等)。初步之工作規畫參考附件 3。

12/7 行程自英格蘭到瑞士

12/8

本日主要工作為討論 AMS-02 中有關 GDAQ 之設計工作進展，內容如下：

(1) Mike Capell 把 AMS-02 Electronic 部份做範例說明(參考附件五)，其中有關本院生產之電子模組包含 Traker，TRD 及 DAQ & Trigger，與七月份之會議結論無甚大差異，另外三所八組李銘誌所提供之 JSBC 規格，他們也把 Review comment 提出說明，並將在下次視訊會議中討論(參考附件六)。

(2) 林志勳說明 AMS Wire 目前設計之現況，並已經完成 Loop-back 及 communication test 之初部功能，已帶回此部份之 VHDL code 及詳細電路，並可以做為 JIM 設計 AMS-Wire 之參考，亦可同時相互 debug 看是否有不完善之處。

(3) Dr. Kuanny 報告 AMS-02 Based Test 之初部結果(已在 GSI Bultien 中發表)，其中 PCI 9080 已確定 Latch-up 過高，無法使用 PC-750 及 PPI 700 因沒做功能測試，故可能會在明年再做 Beam Test，其它 CSIST 之測試零件，均有不錯之結果，並可當 JMDC 設計之參考。

(4) 蔡旭東提報 MDC 之研究，其中主要是說明 JSBC 之建議方塊圖(與本所所提之差異)，蔡博亦開始設計 JIM 中之 PCI 與 AMS-Wire 之測試 PCB，PCI 與 HRDC 之 PCB，同時亦

提出修改之架構，希望將 CAN bus 放在 JSBC，另外 AMS-Wire 與 HDRL / RS422 各用 PCI，此點將會與本所 JSBC 設計人員討論。

(5) 下午主要由本所提出 PDR Review 資料，包含 JSBC，JBU 及 JIM-CAN 三部份，其中 JSBC 及 JBU 因有詳細資料，故基本架構已有共識，將會進行下一步詳細設計，但 JIM 因只提供 CAN 部份，CERN 建議用 Intel 之 Chip，不必再自用 FPGA 設計 CAN Controller，此點將與五組討論，至於 PCI 部份，若我們能設計出通用型之 FPGA 版本，則大家均可使用，此點原則同意，由於缺少 AMS-Wire 及 HDRL 之 PDR 資料，因此此項工作將會再與八組討論未來發展。

12/9-12/10 返程。自瑞士日內瓦到桃園。

五、 社交活動

1. 12 月 4 日晚餐後漫步至魯汶大學校區，各學院之建築物均為 16、17 世紀之 Model，嘆為觀止。
2. 12 月 7 日早上參訪劍橋大學各學院如三一、King 及 Queen 等，並駐足陳之藩教授所寫劍河倒影中之劍橋。
3. 12 月 8 日下午參訪 CERN 之 L3 加速儀(正進行拆除，我們是最後一批訪客)，中研院同步輻射中心陳建德院士亦同行。

六、 建議事項

1. 執行經濟部科專案需要與國外廠商討論及參訪之次數較多，而本院出國必須在一年前報部，若有臨時要參訪之事宜，則受限於名額及地區等因素，造成工作上之困難。建議對執行經濟部科專之出國應給與彈性，如名額及次數不必在一年前決定（未卜先知？），而依任務需求而定。

2. 本次公差任務受限於日數額度，一週內參訪三國四廠，轉機五國，行程緊湊，倍極辛苦。為使出國人員有意願全力以赴，而無後顧之憂，建議平安保險由 400 萬提高到 1000 萬元，以防萬一。

WB-CDMA/WLL Base band chips set (FPGA-based) Design and Implementation

Document Status

Version	Author	Document Status	Issue Date
V1.0	M. Dieudonné	Preliminary	December 12, 2000
V1.1	M. Dieudonné	Preliminary	December 13, 2000

Distribution List

Name	Company
Hao Jinchi,	CSIST
Yung-Tzu Ting,	CSIST
Kwo-Jyr Wong,	CSIST
Allan Lee,	MITS
Nico Lugil,	Sirius
Lieven Philips,	Sirius

Document Number: SC027003/002

1. System Requirements

- [illegible] (WLL) system based on 3GPP Release of Dec.1999.
- User data rate: 64 kbps with [illegible] up to 384 kbps.
- Network capacity of at least 1 BTS and 2 SS.
- Support of BTS and SS mode by the same baseband hardware by "on-the-fly" reconfiguration of the L1 hardware by the microcontroller subsystem.
- Programmability and control performed by [illegible] or ARM9-based microcontroller subsystem.
- FPGA-based implementation.
- Complete L1 hardware and software.
- L2/L3 interface code for ARM9.
- L1 source code and PHY-MAC interface C source code as part of the deliverable.

2. System Specification

2.1 General

Radio Access	3GPP Release Dec. 1999 W-CDMA as reference
Duplexing	FDD
Chip Rate	Programmable from 1.2288 till 7.68 Mcps with 3.84 Mcps as standard parameter
Data Modulation	UL: Programmable BPSK/QPSK with BPSK as standard parameter DL: Programmable BPSK/QPSK with QPSK as standard parameter
Spreading/Modulation	UL: Programmable BPSK/QPSK with QPSK as standard parameter DL: Programmable BPSK/QPSK with QPSK as standard parameter
Spreading Codes	RAM-based fully programmable OVSF codes and Walsh codes, length 4 ~ 512.
Scrambling Codes	Based on programmable Gold Code generators, with up to 42 taps polynomials
FEC Interface	[illegible] 4 soft bits, I and Q
Frame Length	Programmable in #slots per frame, with 10 ms as standard frame duration.
Slot number per Frame	Programmable from 1 till 60 with 15 slots/frame as standard parameter.
Power Control	UL: Open loop; SIR-based slot-based closed loop power control with 80 dB range, step size = 1 dB; outer loop control. DL: SIR-based slot-based closed loop power control with 30 dB range; step size = 1 dB; outer loop control. Independent I and Q power settings, with digital setting range at least 20 dB, and resolution = 0.1 dB.
Detection	Coherent detection in UL and DL; detection CPICH-aided or aided by Dedicated Pilot bits (programmable between the 2 options). Programmable Pilot filter over at least 4 slots.
Diversity	Rake based receiver, with MRC, thresholded zero-forcing, observable energy measurement per finger.
Subscriber Station	Fixed station [illegible]

Interfacing with Processor	AMBA based interface.
L2/L3 interface	Via DPRAM-based mailbox.

2.2 BTS Transmitter

Input data	From interleaver via Serial Port
Output to Front End	I, Q at baseband
# transmitter channels	
Configuration	Each of the reconfigurable transmitter channels can be reconfigured as DCH, CPICH, PCH or AICH.
Required minimum ACLR	At least 43.2 dB. Must be demonstrated by simulation result performed with a Fixed point C simulation model according to TS25.101 measurement conditions (relation between the signal power measured after the baseband filter in a receiver that is situated in the desired frequency band and the same signal power for a receiver that is situated in the adjacent frequency band).
Required maximum EVM	At most 2%. Must be demonstrated by simulation result performed with a Fixed point C simulation model according to TS25.101 measurement conditions (square root of the ratio of the mean error vector power and the mean reference signal power expressed as ? %).

2.3 BTS Receiver

Input from Front End	Near baseband I,Q
Output data	To de-interleaver via Serial Port
Allowed Implementation Loss	BER and BLER according to 3GPP TS25.101 pedestrian speeds.
RACH Receiver	Matched filter-based
Rake receiver	4 fingers.
Rake specification	MRC, thresholded zero-forcing, observable energy measurement per finger.

2.4 SS Transmitter

Input Data	From interleaver via Serial Port
Output to Front End	I, Q at baseband
# transmitter channels	1 reconfigurable
Configuration	The transmitter channel can be reconfigured as PRACH or DPDCH/DPCCH
Required minimum ACLR	43.2 dB. Must be demonstrated by simulation result performed with a fixed-point C simulation model according to TS25.101 measurement conditions (relation between the signal power measured after the baseband filter in a receiver that is situated in the desired frequency band and the same signal power for a receiver that is situated in the adjacent frequency band).

Required maximum EVM	2%. Must be demonstrated by simulation results performed with a fixed-point C simulation model according to TS25.101 measurement conditions (square root of the ratio of the mean error vector power and the mean reference signal power expressed as ').

2.5 SS Receiver

Input from Front End	Near baseband I,Q
Output Data	To de-interleaver via Serial Port, I, Q on 4 soft bits.
Rake receiver/searcher	4 fingers
Configuration of finger	Programmable as searching finger or tracking finger (no specific searcher block).
Rake specification	MRC, thresholded zero-forcing, observable energy measurement per finger.
Maximum Rake time span	100 chips
Measurements	SIR on DPCCH Dedicated Pilot bits.
AGC Control	80 dB range with 60 mV per step.
Allowed Implementation Loss	BER and BLER figures according to 3GPP TS25.101 pedestrian.
SCH Acquisition	Number of slots programmable between 8 and 32 with 16 as standard value. Hardware-assisted (Matched filter and correlator bank) Cp and Cs acquisition. Thresholded maximum selections.
Match filter length	256 chips
Searcher Speed	Refresh rate (search over 100 chips span with 0.5 chips resolution) of 2 possible options: matched filter based search and finger-based search.

3. Payment Conditions

To Be Defined.

4. Acceptance

Prior to the kick-off meeting of the project, a test plan will be defined . Acceptance of the delivery will be defined as compliance to the test plan. This compliance will be demonstrated at Sirius Communications premises, in the presence of CSIST engineers who need to approve.

5. Details on delivery

As part of the delivery, the following services are offered:

- Insight will be given to CSIST in the algorithms used in the SS and BTS modules with flowchart or state diagrams

[illegible]

. In this way it is avoided that the IP included in the FPGA setup is a black box only. This will allow the introduction of changes after the delivery (changes suggested by CSIST which can be implemented by Sirius Communications – conditions To Be Defined).
- Training of CSIST engineers on parameterization/reconfiguration of the setup;
- RT-VHDL of the peripherals hardware;
- [illegible] VHDL codes of FPGA based on mutual decision [illegible]
- C source code of the L1 software for the ARM9;
- C source code for the L2/L3 interface software.

6. Guarantee

For a period of 1 year after the delivery, Sirius Communications will provide support and maintenance for a maximum of 1 support engineer on average. [illegible]

TALITY

3G Infrastructure

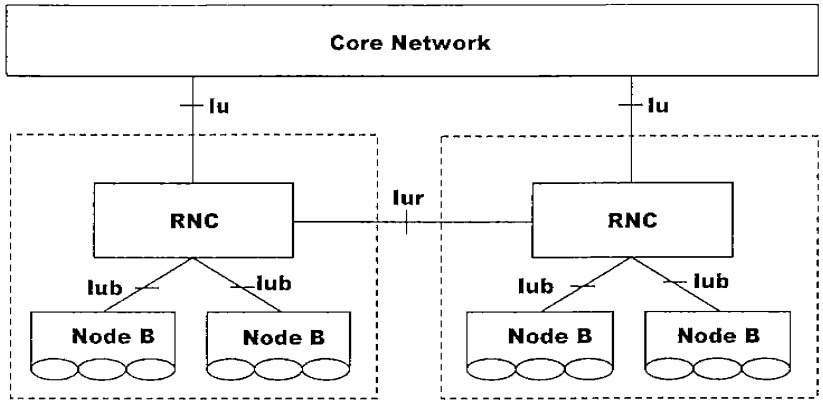
November 5th 2000

Wireless and Multimedia Design Group

Projects and skills summary

- UMTS RNC Development project
- Experience and Capabilities

Background



Our client, a major European telecoms equipment manufacturer, was in the early stages of the development of the RNC component of a UMTS basestation.

Tality was able to satisfy the requirement to strengthen the team with domain experienced engineers. We have worked with the client for more than 18 months.

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RNC development project

Involvement in Development Process

- Requirements analysis
- Interface specification and design
- Software architecture
- Call control software
  - use case and scenario development
  - internal software architecture
  - state machine design
  - implementation
  - test
- Definition of test solutions
- Project management

TALITY

Standardisation and Interface Definition

- recognised the significance of the emergence of 3rd Generation Cellular standards early
- our experts have been actively involved in the 3GPP standardisation meetings, contributing on radio access network, baseband, protocol and radio issues
- in-depth understanding of the UMTS standards proved invaluable in working with the customer to define and implement the external interfaces of the RNC
- some of our work has been input into 3GPP working groups aimed at the standardisation of the interfaces.

TALITY

Skill sets

- RNC design lifecycle with particular emphasis on the call control software and the Iu, Iub and Iur interfaces
- Advanced development tools and methodologies
- RNC system architecture
- ASN.1, and the encoding and decoding of UMTS messages using state of the art ASN.1 tools
- architecture, state machine design, implementation and test of call control software

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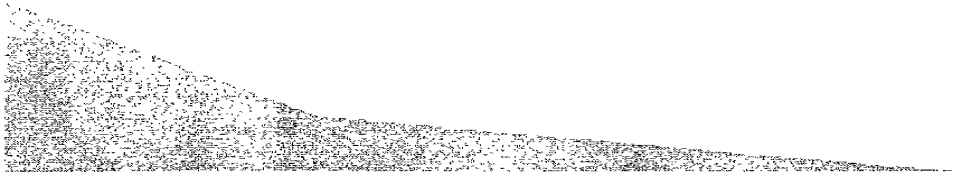
TALITY™

RNC Development Approach

UML & Rational Unified Process

- Working with client to put into practice new methodology:-
  - Model-centric development
  - Use-Case Driven
  - Iterative, Risk-aware development planning
- Using leading-edge development tools to address aggressive time-to-market goals
  - Rose Real Time provides full graphical design and test environment
- Analysis Model in Rational Rose allowed high level architecture to be formulated independently of the implementation

Service Control Context



Use Case Analysis

- Service Control Use Cases
  - Role
    - Structured statement of Service Control "black-box" requirements
  - Size
    - 125 Use Cases identified from full specification
    - Around 30 selected from 125 are required for initial release

TALITY

Analysis Model

- Classes have public operations/external events
- private operations identify important internal algorithms

State Machine Modelling

- Interesting Analysis Classes have state-based behaviour and therefore FSMs inside

Static Architecture

- Relationships between classes are modelled in UML and documented in class diagrams

Scenario Descriptions

Analysis Model to Implementation Model Mapping

- Classes in the AM represent logical entities which map onto the implementation

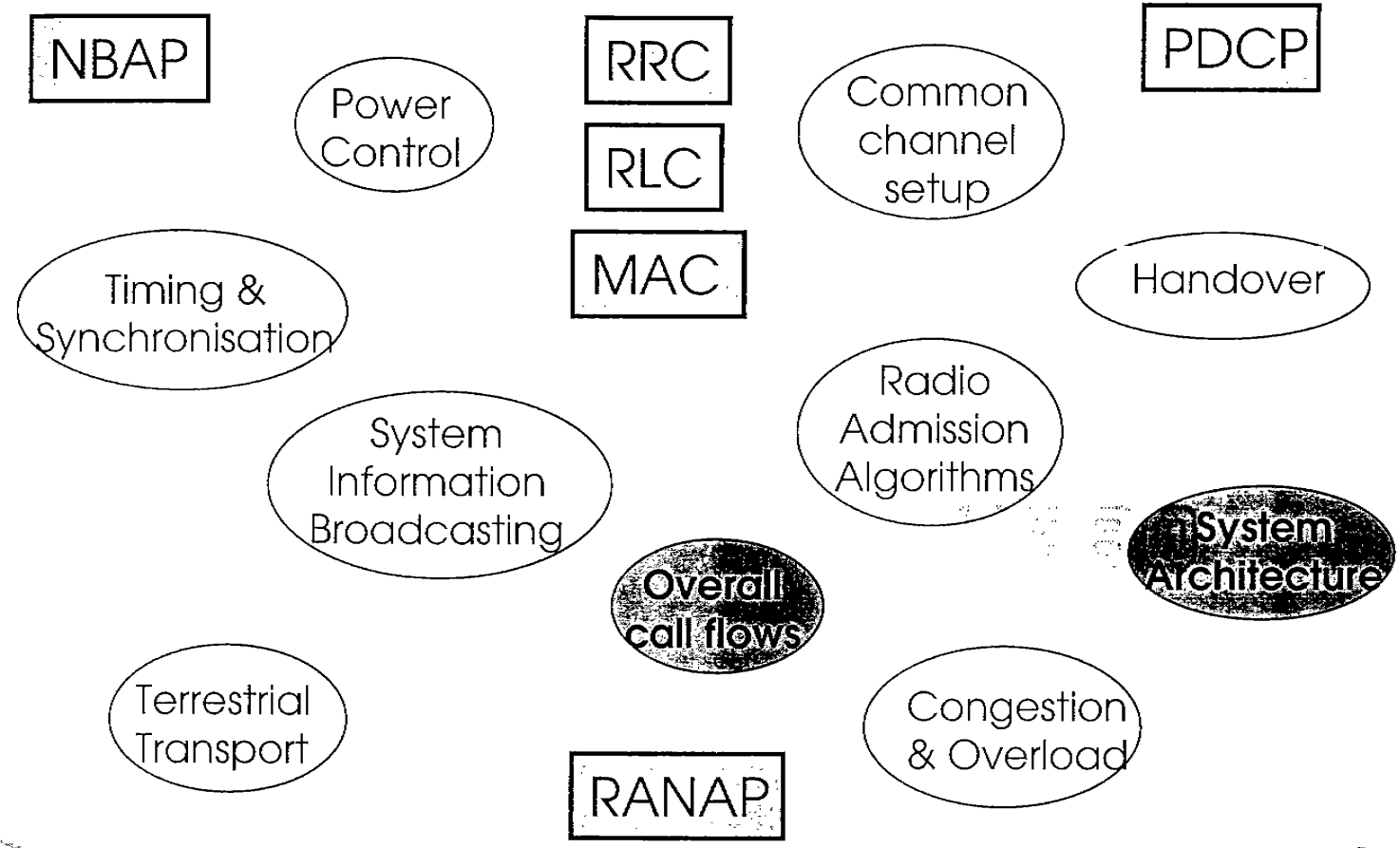
Summary

- Plus Points
  - Use Case based design provides sound basis for flexible project management
  - Iterative Approach allows early validation of the architecture
  - Graphical tools do indeed offer prospect of real productivity gains
- Negative Points
  - Tools are still evolving and many practical issues can hinder progress in large, multi-site teams
  - Model Validation in Rose is difficult, because it does not product executable output

TALITY™

3G infrastructure experience and capabilities

Specific Areas of RNC Expertise



TALITY

Complementary skills

- Digital Cordless
  - DECT, PWT, PHS & proprietary systems for Cordless & Radio Local Loop applications
- Digital Cellular
  - GSM 900/1800/1900, GSM-EDGE/GPRS, IS-95, IS-136 & Satellite
- Wireless Connectivity
  - Bluetooth & HomeRF/SWAP
  - Wireless Information Devices - EPOC (Symbian)
  - 802.11 & HiperLAN wireless networking
- Location & Paging
  - GPS, ReFLEX
  - AMR
- Multimedia
  - Digital TV solutions for Terrestrial, Cable & Satellite
  - Multimedia and digital imaging

TALITY

Summary of 3G Infrastructure Capabilities

- system architecture design
- engineering teams experienced in the complete development flow for call control software within the RNC, from requirements capture through to implementation and test
- expertise in 3GPP standards and ASN.1
- development of operations and maintenance (O&M) systems
- links into IP transport and other network infrastructure layers
- establish design methodologies and tools to seed these large software projects

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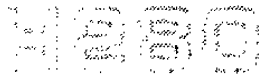
Example of State Machine Implementation

- Finite State Machine design is integral with code in RRT



附件三

TALITY™

Development of elements of 3G WLL for CSIST

Gregory Luxford & Frances Thomson

Background (1)

- CSIST are interested in developing a WLL based on 3GPP W-CDMA technology.
  - Provide modern communication infrastructure for Taiwan
  - Transfer knowledge of leading-edge technology to Taiwan's industry.
- CSIST seek partners to develop elements of a 3G WLL.
  - Development is an enormous undertaking.
  - Managed team of engineers to complement their own activities.

Background (2)

- Tality are in a unique position to assist.
- Already conducted study of 3G WLL for CSIST (Burrito).
  - Experience of WLL developments (Ionica)
  - Experience of RNC development (Diamond/Solitaire) network company
- Currently developing SDL models of RLC & RRC for CSIST (Cheiron).
  - Roadmap to complete Access Stratum in 2001.
- Large investment over past 3 years to foster a multi-disciplined team
  - L1, L2 & L3
- Significant experience of 3G
  - training, attend standards bodies, internal R&D, develop IP portfolio

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Key Requirements

- CSIST are interested in developing 3G products, starting with WLL applications:
  - Initially: CS voice & PS data
  - Ultimately: PS (IP-based) voice & data
- CSIST require a complete software architecture for a WLL:
  - RNC
  - Node B
  - UE
- CSIST want the SW solution
  - modelled in SDL
  - efficient tested C code

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Tality Approach

- We have identified a set of tasks which can be done to fit into next year
  - based on bottom-up approach only.
- We would welcome guidance from CSIST about what their priorities are
  - can revise this to realize CSIST's short-term goals.
- We would like details of CSIST's HW platform so that we can estimate timescales and costs for porting of C code.

Business Issues

- We would like to understand how CSIST can manage projects which take longer than one financial year.
- We request CSIST to document the details of their procurement and contracts process
  - need to ensure payments/delivery terms are agreed up front
  - need to ensure that all parties are agreed on the complete contractual terms before work starts

Partitioning

- CSIST will purchase non-3G-specific elements (e.g. TCP/IP) direct from a third party vendor (more cost-effective than own development).
- Care is required in partitioning the system to ensure third party elements can be integrated easily.
  - Design methodology
  - Implementation
  - Interfacing (ideally minimise umber of interfaces)
  - Integration
  - Test strategy

TALITY

Tality Solution

- As a full 3G WLL development would take 2-3 years to complete, Tality proposes:
  - Most 3G elements are split (e.g. development vs. porting) into work packages of less than 1 year by duration, to fit CSIST's financial year. Some will be done in 2001; some deferred to following years.
  - Other 3G elements which cannot be completed within a year (i.e. RANAP & NBAP) will be discussed by Tality & CSIST to determine a strategy to complete them.
  - Define projects by level of effort , since CSIST's own budget for work is allocated by government annually.
  - Some agreed mandatory deliveries; some additional work that is limited in scope by the remaining budget

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Project Scope and Responsibilities: Tality SDL

- Project management and peer development of SDL to 3GPP specifications (March 2000) of:

	RNC	NB	UE
• RRC, RLC & MAC	x	x	x
• PDCP	x		x
• IWU	x		x
• RRM	x		
• FP	x	x	
• Iu-UP	x		

- Additionally the SDL models of the RRC, RLC, MAC & PDCP will be integrated at this stage.

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Project Scope and Responsibilities: Tality C Code

- Project management, peer development of platform independent C code to 3GPP specifications (March 2000), and integration of:
  - RRC
  - RLC
  - MAC
  - PDCP

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Project Scope and Responsibilities: CSIST

- Provide product requirements (for each element in the table) to Tality covering:
  - functional overview
  - features to be included/excluded
  - other constraints

	RNC	NB	UE
• RRC, RLC & MAC	x	x	x
• PDCP	x		x
• IWU	x		x
• RRM	x		
• FP	x	x	
• Iu-UP	x		

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Project Scope and Responsibilities: CSIST

- Development to 3GPP specifications (March 2000) of:
  - PHY
- Delivery of MAC/PHY interface specification
  - CSIST will implement own interface consistent with TS25.302 specification (March 2000)
- Provide delivery dates to Tality for all deliverable items.

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Project Scope and Responsibilities: CSIST

- Purchase of suitable third party software for:

	RNC	NB	UE
• LAPD (AAL2/AAL5)	x	x	
• E1 (ATM)	x	x	
• CC & MM	x		x
• SM, GMM & LLC	x		x

- Tality are positioned to assist in this, as we:
  - can advise about choice of third party software
  - aim to form an alliance (access & integration) with a producer of CC, MM, SM, GMM & LLC
  - plan to make vendor selection by end of January 2001

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Deferred Scope and Responsibilities: Tality

- RANAP & NBAP do NOT form part of the proposed work at this stage. However they are are a natural extension to it, and could form the basis for future projects.
- Other work could include:
  - update SDL to more recent versions of the 3GPP specifications (parts of this will be done as internal R&D and access will be granted for an upgrade fee)
  - integrate SDL modules with each other (where not done already)
  - encode in C as platform-independent modules (where not done already)
  - integrate C modules with each other (where not done already)
  - port C modules to selected hardware platforms
  - integrate C modules with third party software

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Deferred Scope and Responsibilities: CSIST

- Activities for CSIST to consider:
  - selection of hardware platforms for each part of system
  - approvals
  - trials
- Tality would be happy to quote for supplying consultancy services in these areas.

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IP Elements

- Tality IP blocks (SDL & C code to March 2000 specifications) needed for project:
  - RRC — extended functionality
  - RLC
  - MAC
  - PDCP
- Third party IP blocks needed for complete 3G WLL project:
  - AAL2/AAL5 — Trillium or other
  - ATM — Trillium or other
  - CC & MM — Tality's partner or other
  - SM, GMM & LLC — Tality's partner or other
- Tality can supply extra services in this area if required.

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Deliverables

- Phase 1: Definition
  - Documentation: functional spec, interface spec & test spec
  - Management strategy: project plan, quality plan, risk analysis, scope priority
- Phase 2: Implementation
  - SDL models for all elements, with peer test scripts and results
  - PC-targeted C code for MAC, RLC, RRC and maybe PDCP
  - Documentation: updated functional spec, interface spec and test spec
- Phase 3: Transfer
  - Presentation about design and operation
  - Statement of scope (fixed price, variable scope)
  - Training & support (scope to be agreed)

Dependencies

- Successful completion of the project relies on CSIST providing Tality with:
  - Timely feedback on all communications (e.g. queries, change requests, and acceptance procedures)
  - All data or inputs requested during the project (e.g. interfaces and test harnesses derived from third party blocks)
- Dependencies and slippage will be documented:
  - Dependencies on CSIST will be listed in the Statement of Work
  - Slippage (affecting timescale and /or cost) will be recorded in change orders issued by Tality.

Working Assumptions

- SDL will be produced using Telelogic Tau v4.1.1 or later
- All C code is platform-independent, delivered on PC platform
- Work on purpose-developed elements will start by 1 April 2001.
- Work on licensed elements will start as per current Tality plans.
- All elements will be developed to the March 2000 version of 3GPP specifications. Upgrades to later versions may be available on payment of a licence upgrade fee.
- SDL & C code of MAC, RLC, RRC & PDCP will be integrated.
- SDL models of FP, Iu-UP, RRM & IWU will be developed as initially isolated peer systems (i.e. NOT integrated)

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Schedule Estimate

- Licence availability (SDL integrated systems)

	Duration	Work Start	Licence Available
• RRC full	5 m	Apr 01	Sep 01
• RLC	12 m	in progress	Jan 01
• MAC	6 m	Feb 01	Aug 01
• PDCP	5 m	Feb 01	Jul 01

- Development work (SDL peer systems)

	Duration	Work Start	Work Finish
• IWU	8 m	Apr 01	Dec 01
• RRM	8 m	Apr 01	Dec 01
• FP	6 m	Apr 01	Oct 01
• Iu-UP	7 m	Apr 01	Nov 01

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Schedule Estimate

- Licence availability (C integrated systems)

	Duration	Work Start	Licence Available
• RRC	5 m	Jul 01	Dec 01
• RLC	4 m	in progress	Feb 01
• MAC	3 m	Aug 01	Nov 01
• PDCP	3 m	Jul 01	Oct 01

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Risk Analysis

- Tools do not work as described by vendor.
  - Exercise tools before use on project
  - Develop work around
  - Request vendor to remedy problem
- Tools are working at edge of performance (size or type of task)
  - Upgrade tool (if available)
  - Use compatible alternative (hybrid language/environment development solution)
- Procedures in 3GPP specifications do not operate properly
  - Clarify using later specification (if available) or 3GPP reflector
  - Omit (replace with stub) at discretion
- Others
  - To be determined

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Open Issues

- Select version of 3GPP specifications to which work shall be done (assumed to be March 2000).
  - Revise work estimates if later version of specifications is required
  - In some instances later versions of the specifications will be used at Tality's discretion to resolve ambiguities in the selected version of the specifications.
- Identify mandatory and optional tasks (or agree appropriate proportional split)
- Agree pragmatic approach to mix of SDL & C at low level in design phase.

Commercial Model (1)

- Licensed elements
  - Offered on a fixed price basis.
- Developed elements
  - Offered on **defined level of effort** basis (avoids high premiums associated with the high risk of fixed price developments, and introduces incentive for Tality to complete work efficiently).
  - CSIST and Tality will agree a core set of mandatory tasks, an additional set of optional tasks, and a fixed budget.
  - Tality will complete all mandatory tasks.
  - Tality will use remaining budget (if any) to finance optional tasks, until such tasks are complete or all the budget is spent (whichever happens sooner).
  - Tality will be awarded remaining budget (if any) as a bonus.

Commercial Model (2)

- Invoices
  - Five equal payments.
  - Payment due on first working day of Apr, Jun, Aug, Oct & Dec 2001.
  - Payment terms, strictly 30 days.
- Reports
  - Issued monthly
  - Indicate progress against identified tasks and timescales.
  - Justify deviation from estimates.

Summary

- 3G WLL development is an enormous undertaking. Tality is in unique position to assist.
- Anticipated schedule
  - Full 3G WLL development would take 2-3 years
  - Propose to 'divide and conquer' into manageable blocks that fit with CSIST's financial year.
- Estimated cost
  - In the range $5.0M - 8.0 M (when detailed functionality is agreed a more refined quote can be given)
  - Defined level of effort (DLOE) and focus on most important aspects of tasks.

Next Steps

- Agree scope of project.
  - Identify mandatory and optional tasks (or possibly the proportional split of work for later allocation).
  - Define functionality/scope of each protocol layer in detail.
- Professional Services Agreement.
  - Legal and commercial engagement.
- Statement of Work.
  - Project activities, deliverables and payments.

The purpose of this document is to assist common understanding of project requirements and provide information in support of the budgeting process; it does not constitute an offer to render services.

Estimates of cost and schedule presented here are based upon our current understanding of the project scope and may need to be revised prior to agreement of a formal Statement of Work.

This document was presented to CSIST on 6 December 2000 and is valid for a period of 30 days immediately following this date.

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CSIST WB-CDMA/WLL SYSTEM DESCRIPTION

YUAN TZU TING

NOV. 22, 2000

中山科學研究院
電子研究所

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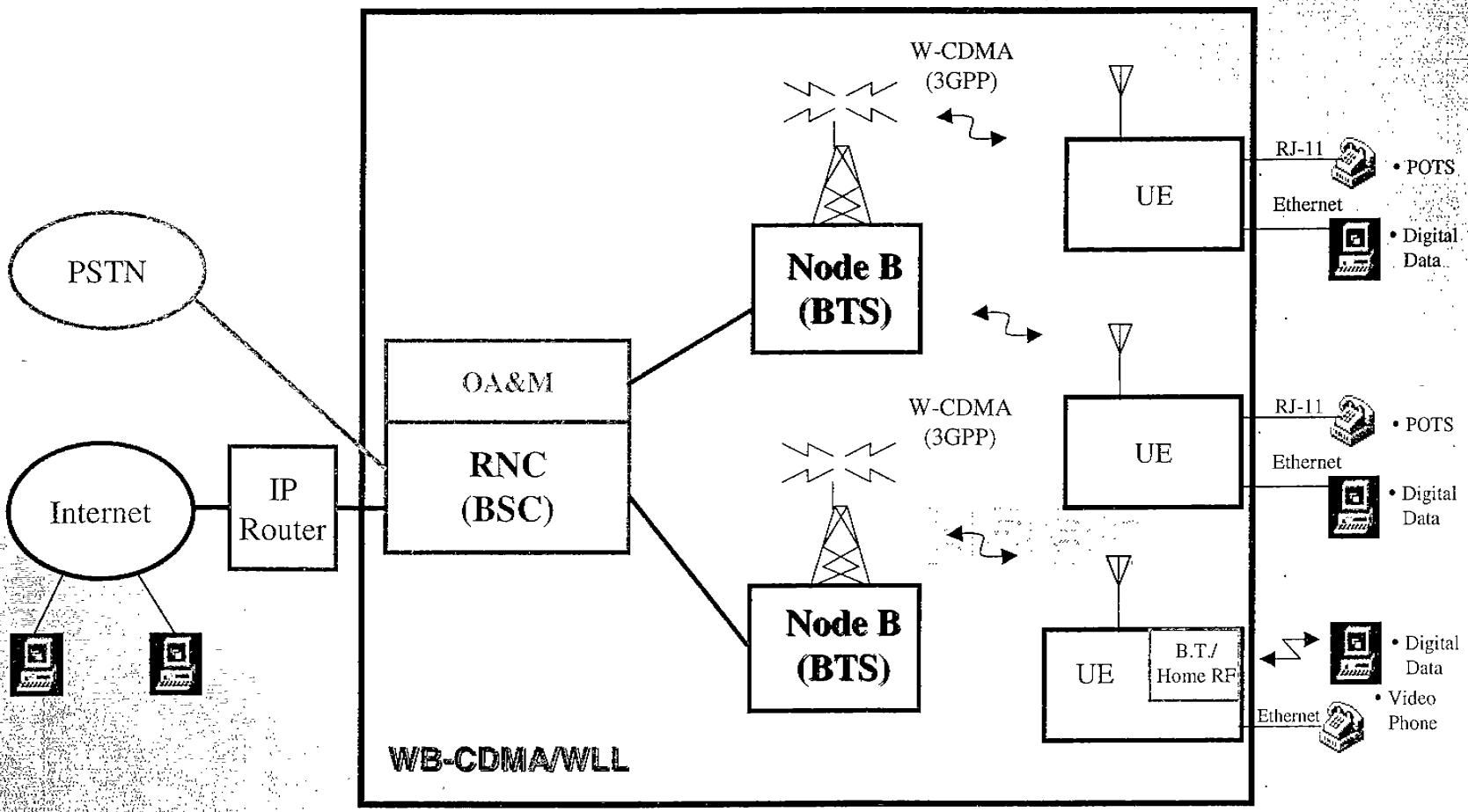
CSIST WB-CDMA/WLL SYSTEM ARCHITECTURE



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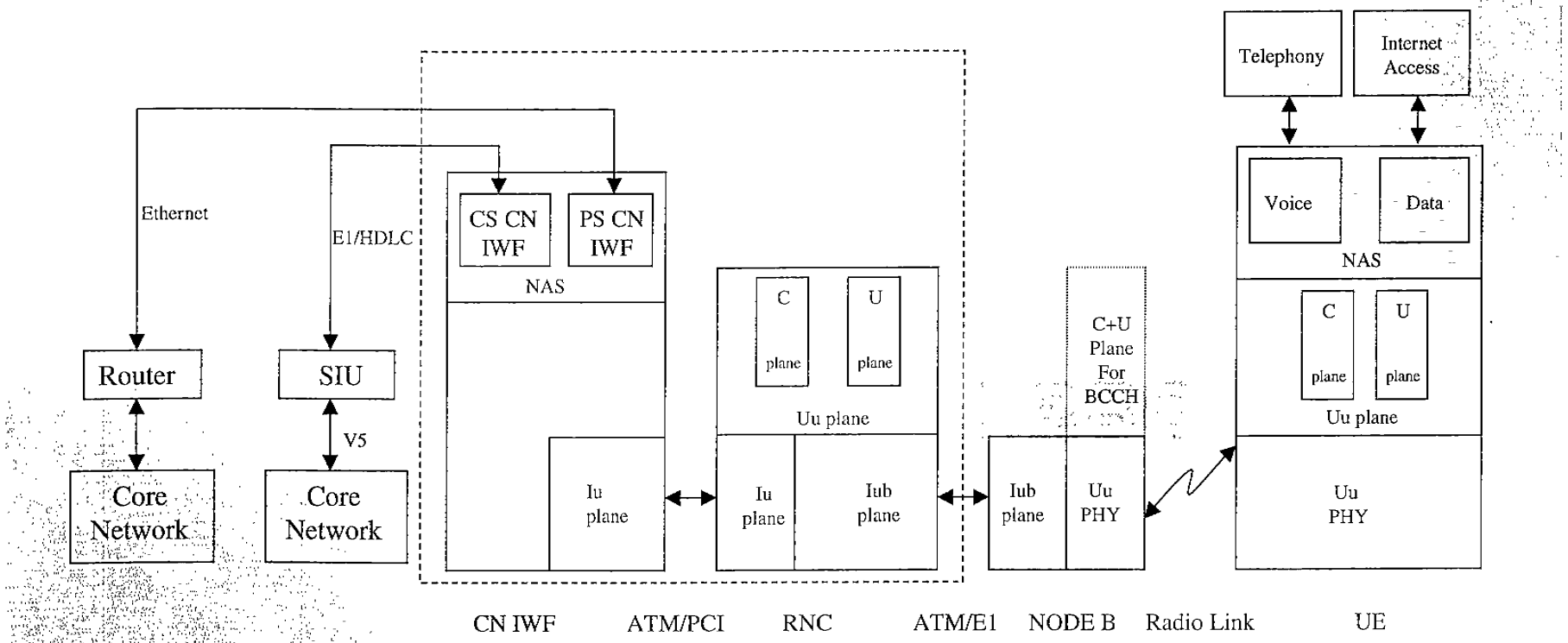
WB-CDMA/WLL SYSTEM SPEC.

Radio Access	3GPP W-CDMA
Freq. Band	◦ Uplink:1850-1910MHz ◦ Downlink:1930-1990MHz
Duplexing	FDD
Carrier Spacing	5MHz
Chip Rate	3.84Mcps
Data Modulation	◦ UL:BPSK ◦ DL:QPSK
Spreading Modulation	◦ UL: QPSK (complex spreading) ◦ DL: QPSK (complex spreading)
Spreading Codes	◦ Channelization code: OVSF codes ◦ Scrambling codes: Long Gold codes
Multiple Rates	Variable spreading factor, 4 ~ 256
FEC	Convolutional code with Viterbi soft decision decoding (K= 9; r = 1/2 and/or 1/3)
Frame Length	10 ms
Slot numbers per Frame	15 (Slot length = 0.667 ms)
Power Control	UL: Open loop; SIR-based fast (1.5 kHz) closed loop power control with 80 dB range, step size = 1 dB; and outer loop control DL: SIR-based fast (1.5 kHz) closed loop power control with 30 dB range; step size +- 1 dB; and outer loop control

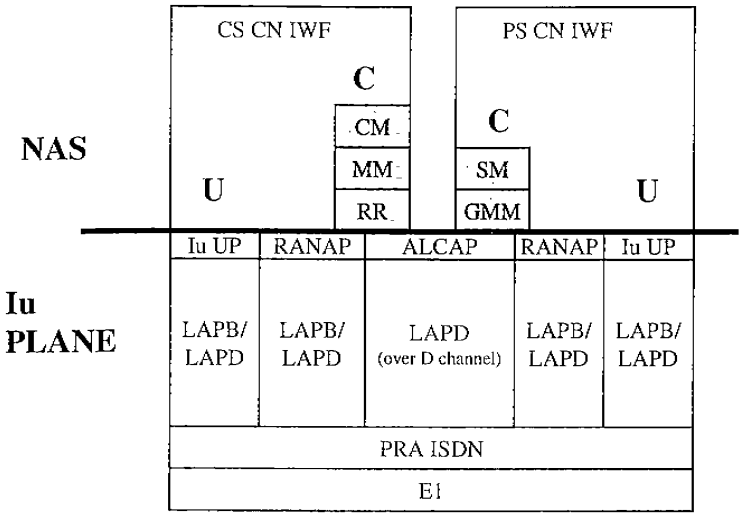
WB-CDMA/WLL SYSTEM SPEC.

Detection	Pilot symbol-aided coherent detection (UL&DL)
Diversity	☞Path Diversity: RAKE receiver with MRC; ☞Time Diversity: FEC and interleaving; ☞Space Diversity: Antenna diversity (UL)
Inter-BTS Synchronous	Asynchronous (without GPS synchronization)
Service Data Rate	☞64 kbps PCM POTS @ BER= 10^{-3} ~ 10^{-6} (FY2001 Target) ☞32 kbps ADPCM POTS @ BER= 10^{-3} ☞Max. 384kbps PCM POTS@BER=10^{-3} ~ 10^{-6} (Design Goal for Tech.Transfer Contract)

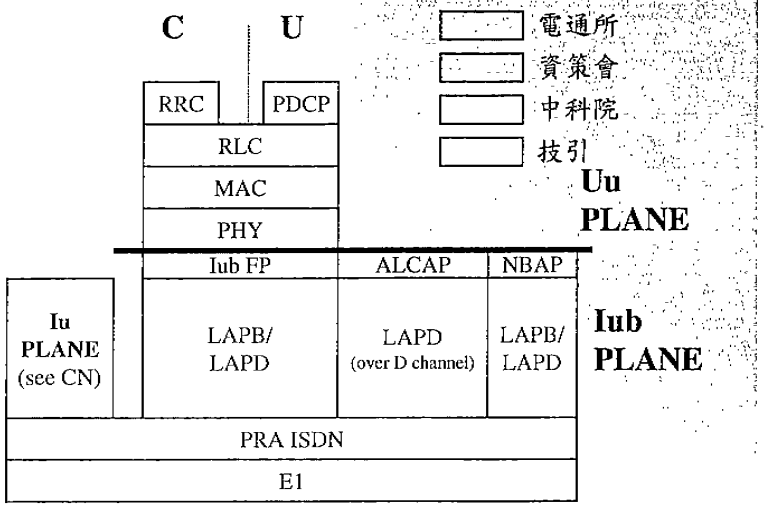
WB-CDMA/WLL 3GPP PROTOCOL ARCHITECTURE



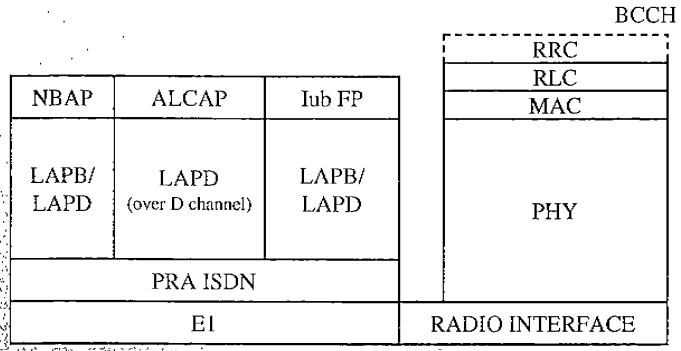
WB-CDMA/WLL PROTOCOL ARCHITECTURE



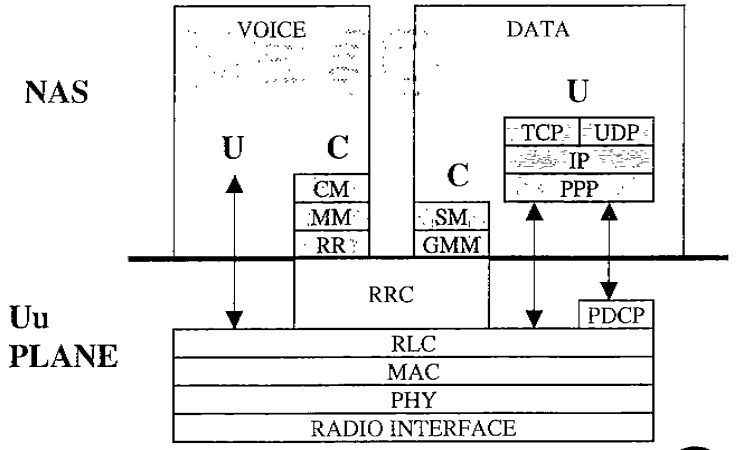
CN (IWF)



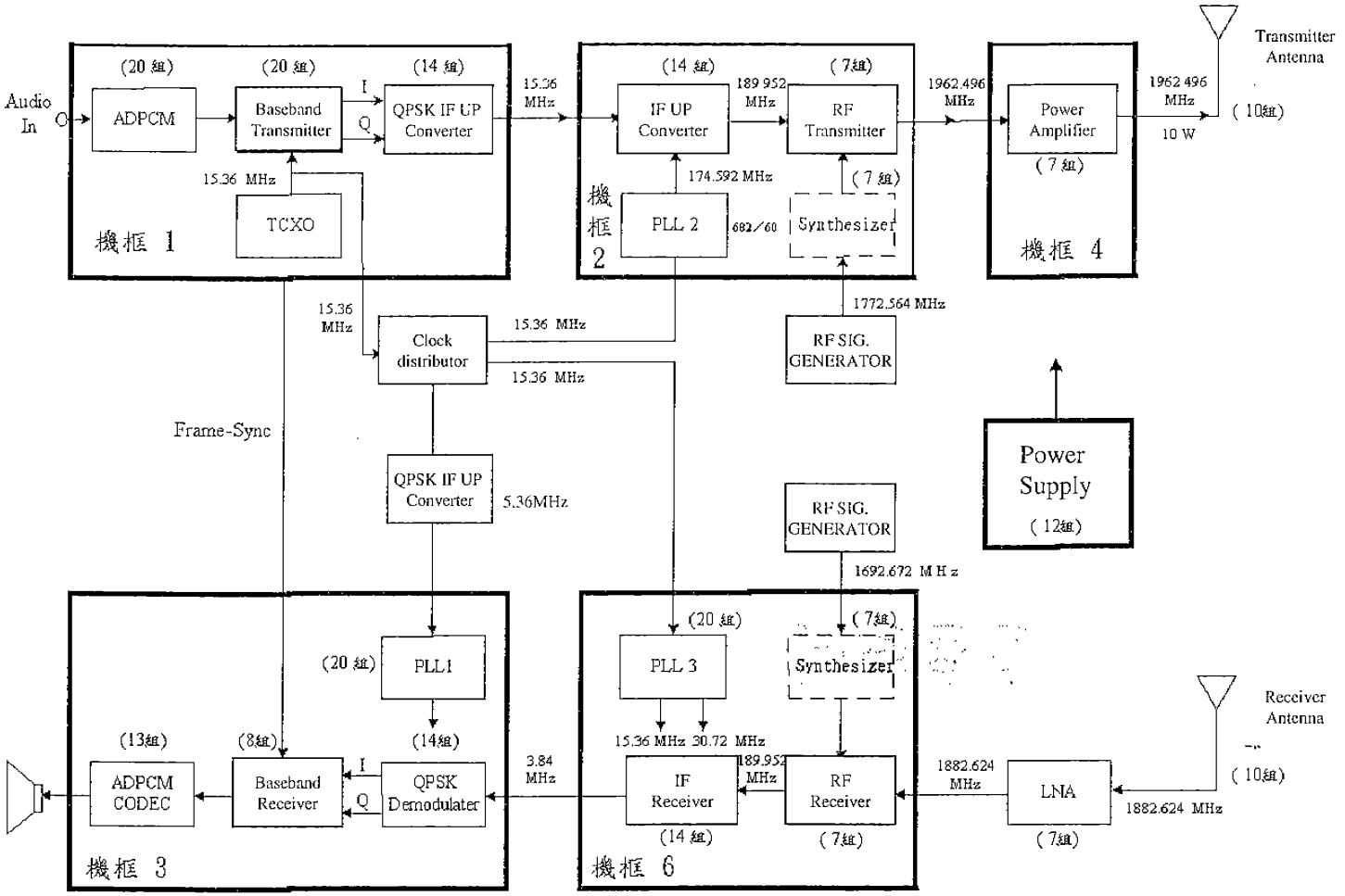
RNC



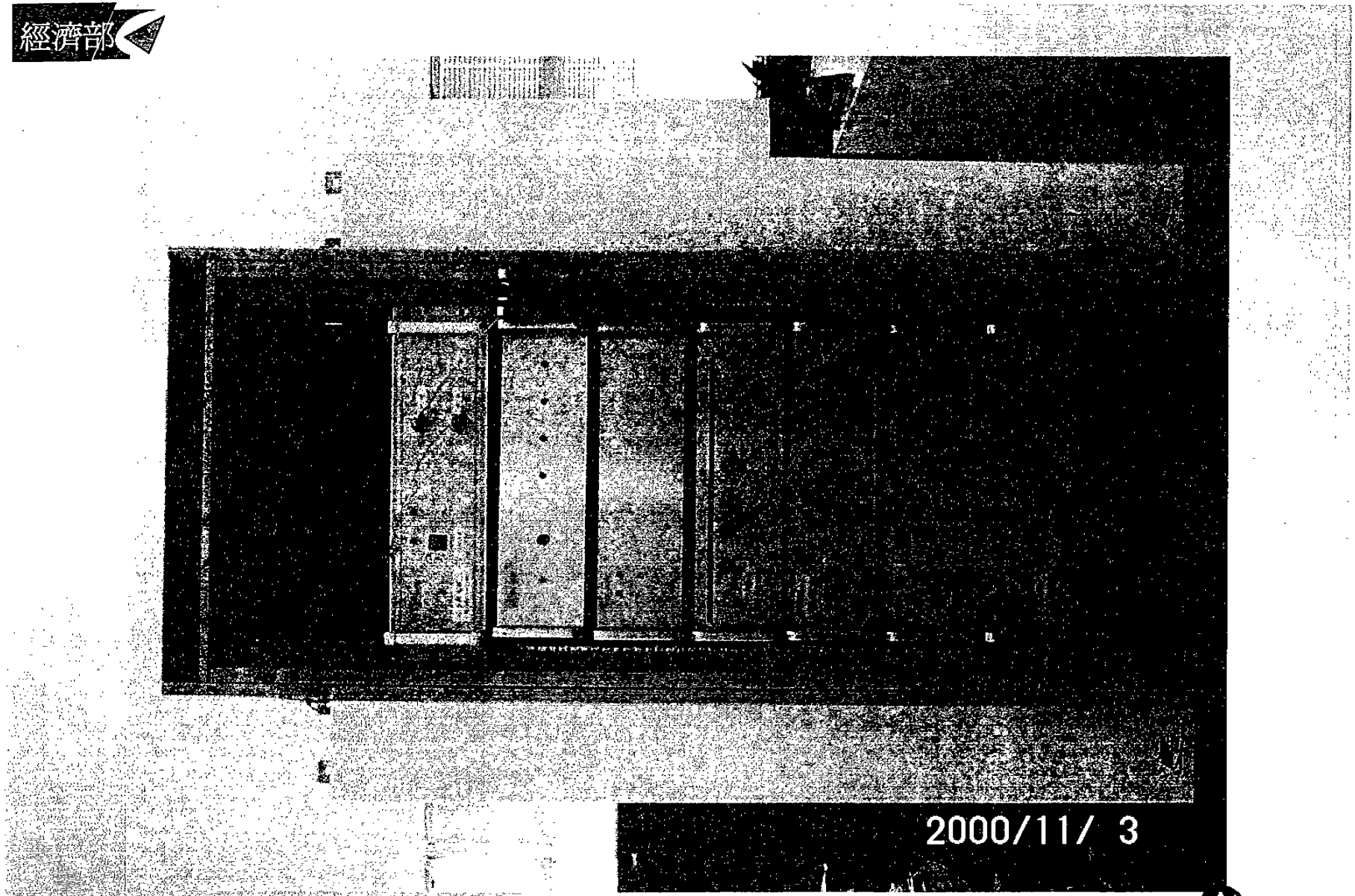
NODE B



UE



ARCHITECTURE FOR BTS(NODE B) DEMO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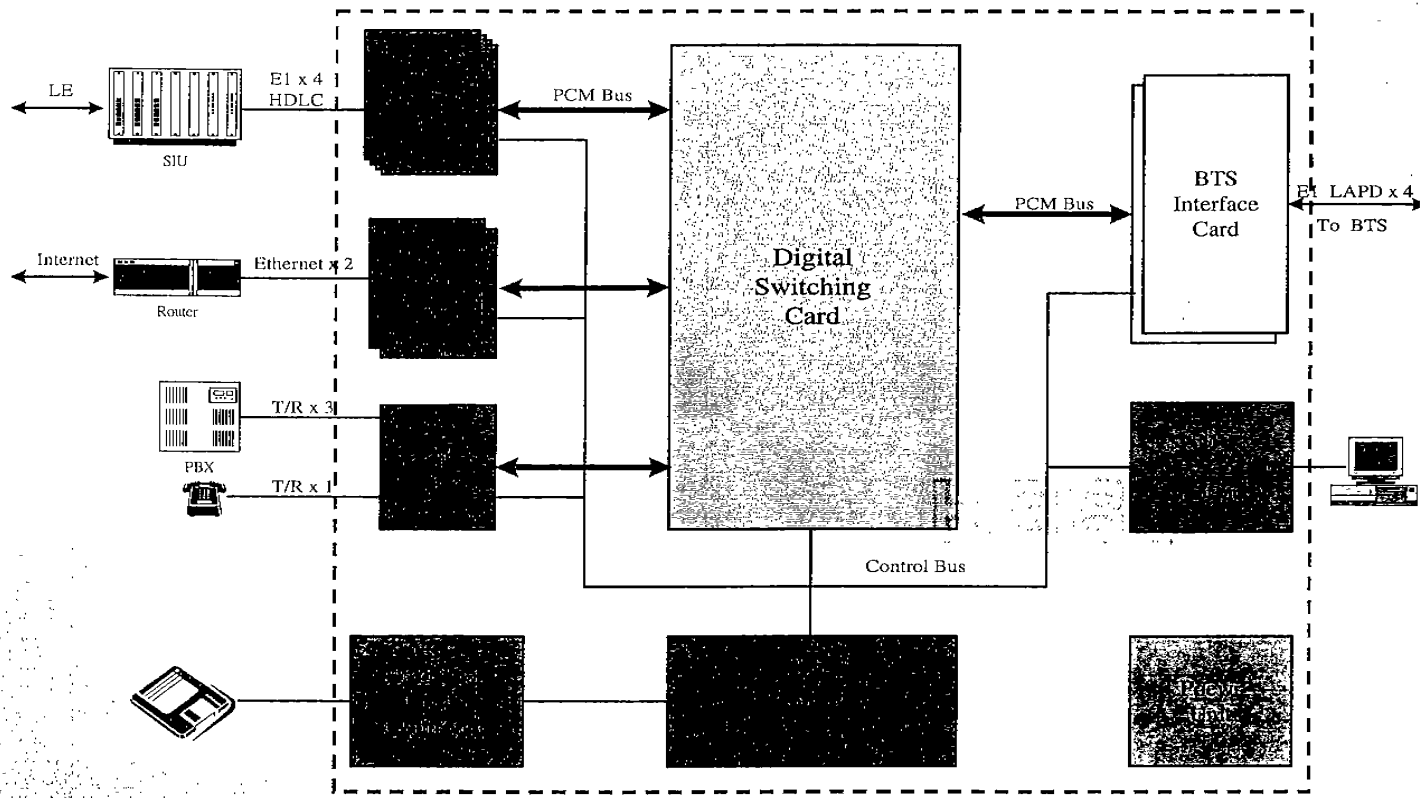
RNC SYSTEM BLOCK DIAGRAM



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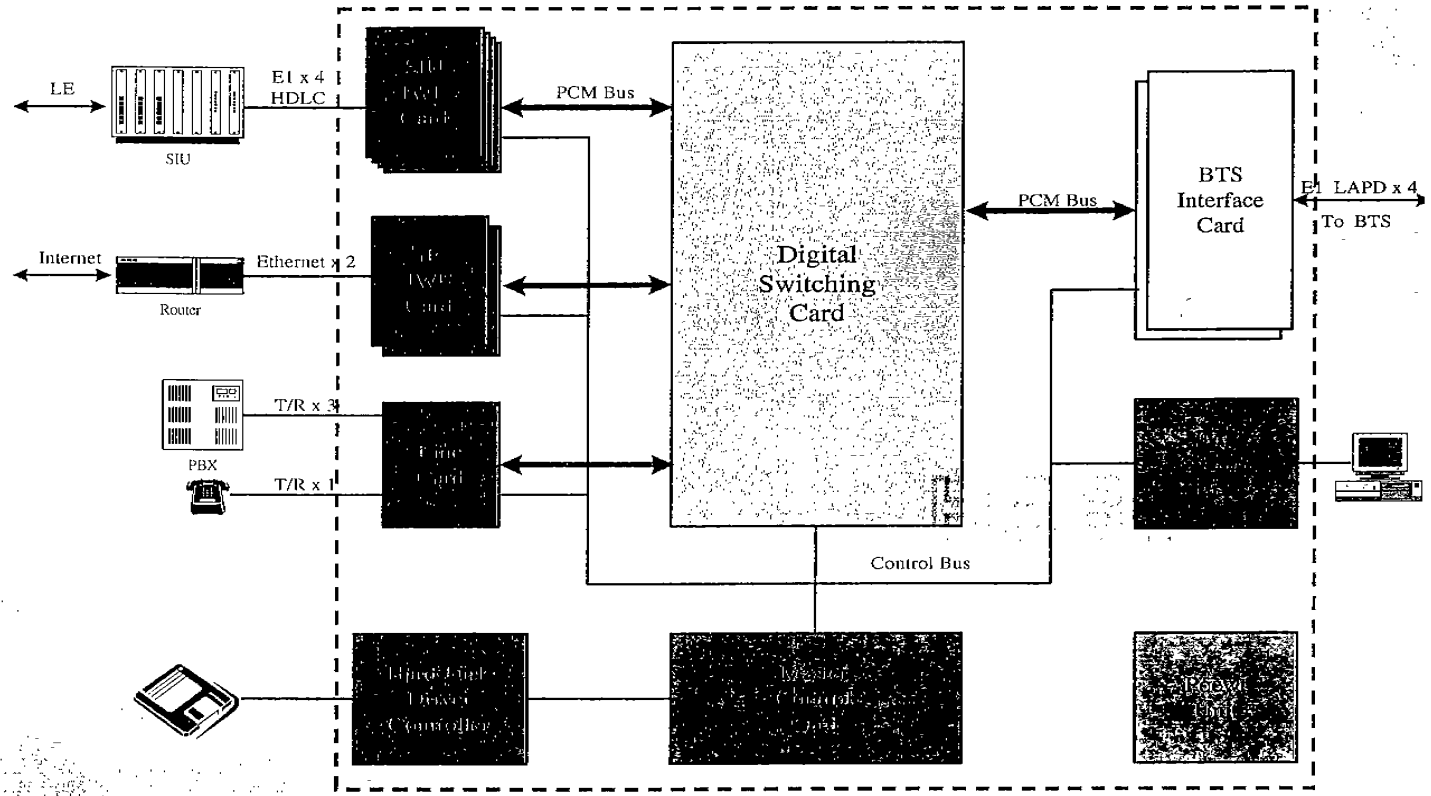
RNC SYSTEM BLOCK DIAGRAM



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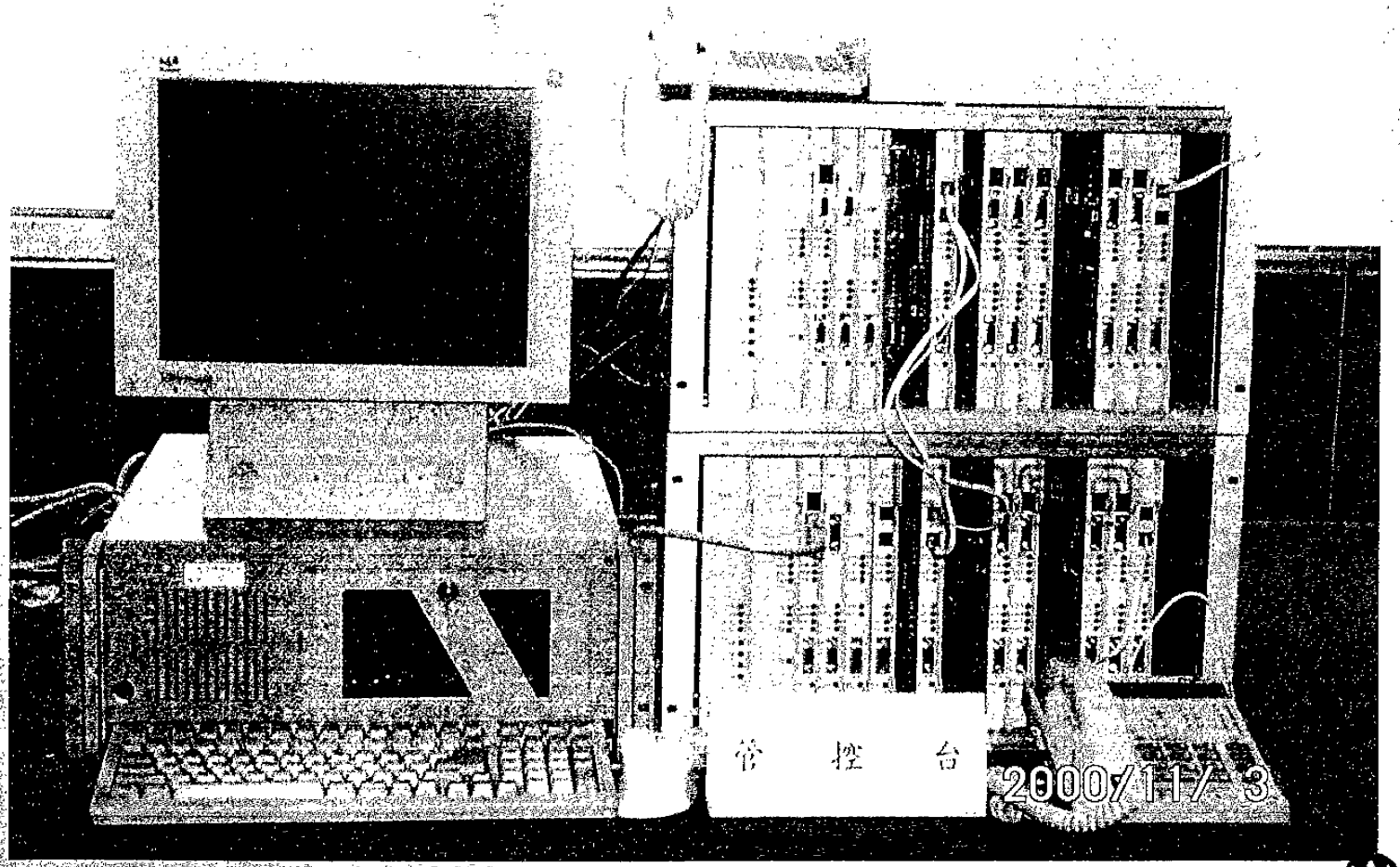
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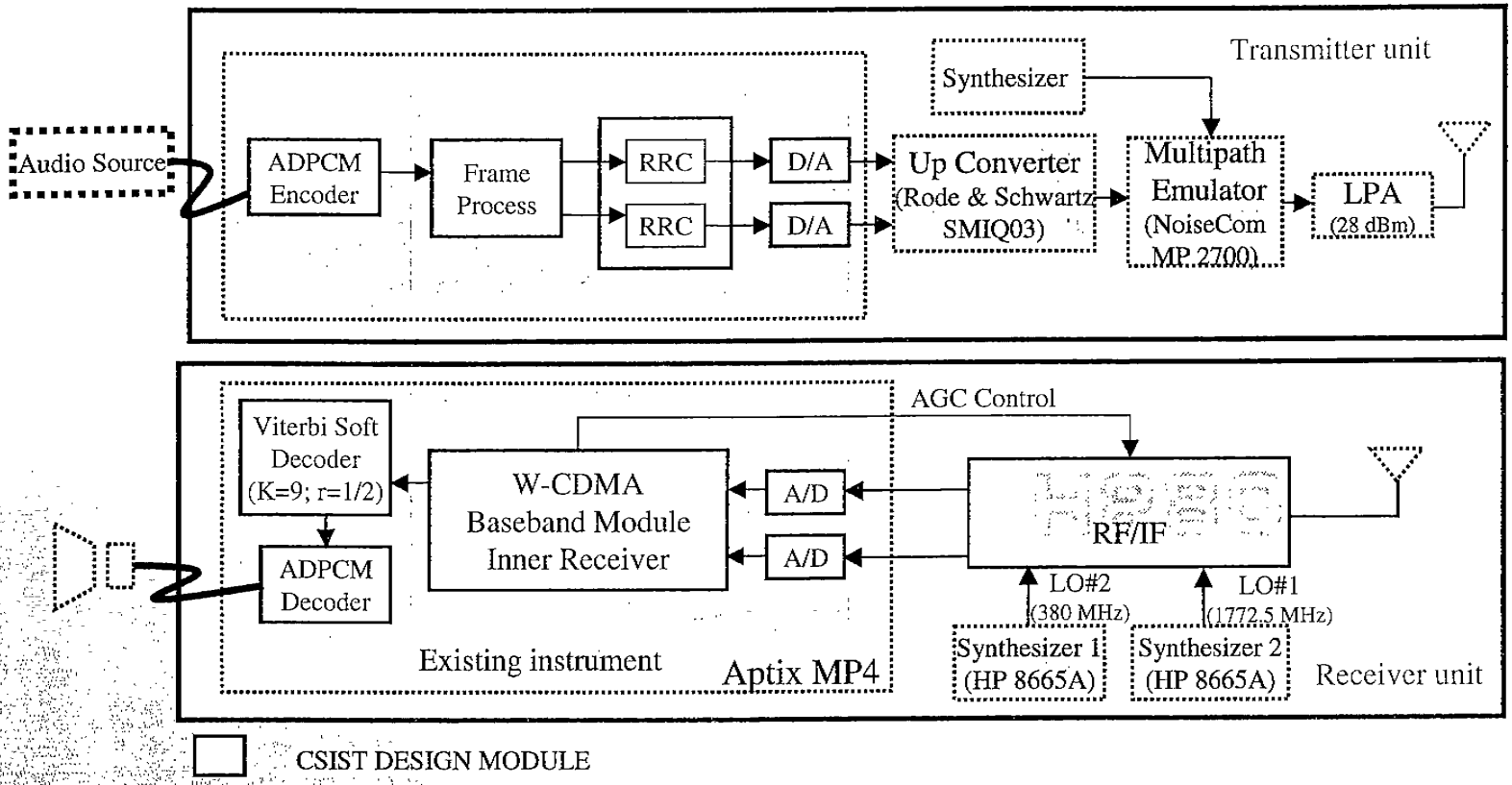
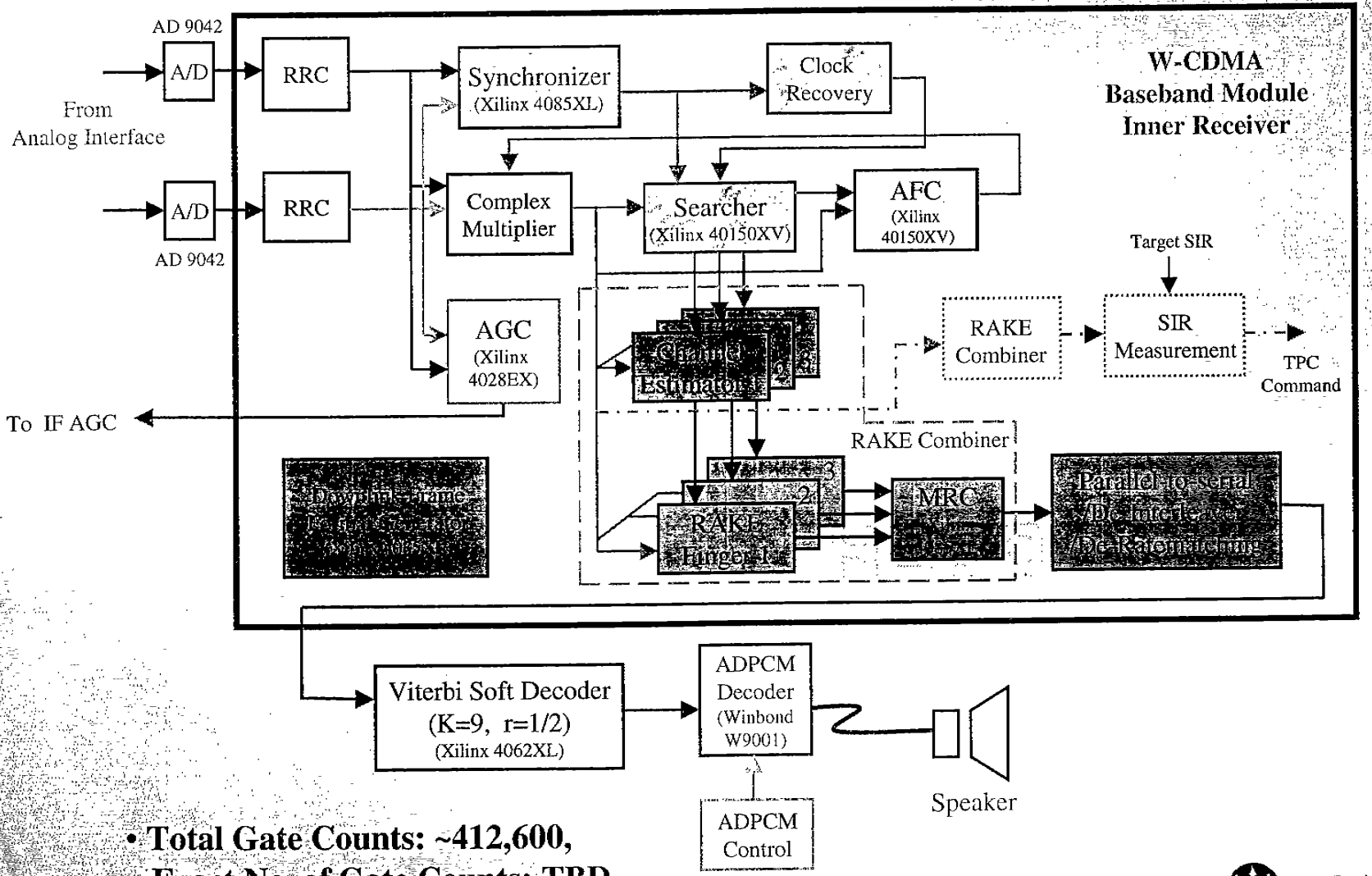
WB-CDMA/WLL UE SYSTEM BLOCK DISGRAM



SS BASE BAND RECEIVER PROTOTYPE SYSTEM



- **Total Gate Counts: ~412,600,**
  Exact No. of Gate Counts: TBD

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DISCUSSION ISSUES

1.The application of Sirius IP Cores for CSIST WB-CDMA/WLL

(1).CSIST Requirement

MS key technology requirements to improve the performance of the Aptix prototype UE

* Searcher and frame synchronizer
* Channel estimator and RAKE receiver
* SIR measurement and power control
* Digital AGC and Dynamic range control
* AFC tracking/PLL

BTS key technology requirements

* RACH (128/256 variable coefficients taps match filter
* Tracking module

(2). Sirius support

* MS (TBD)
* BTS(TBD)

2. Adaptation of CDMAX IP cores from Sirius for WB-CDMA/WLL implementation

*Possibility
*Approach
*Cost
*Schedule

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3.Cooperative development or technical support (transfer) for CSIST WB-CDMA/WLL

* IP core Implementation based on CDMAX for WLL
* Algorithms development for CSIST/WLL
* Implementation of IP cores on Aptix for verification
*Technical support issues during the codevelopment phase

4.Time schedule

* Oct. 2001 WB-CDMA/WLL system demo
* Apr. 2001 Contract signed
* Jan. 2001 RFP completed
* Dec. 2000 Spec. confirmed

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Taiwan market analysis for CDMA (IS95) and W-CDMA

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電子研究所

CDMA 全球用戶數預估

單位：百萬戶

地區/頻段	1998	1999	2000	2001	2002	2003
美國/1800	2.535	5.942	12.246	18.551	24.856	31.16
美國/1900	2.15	3.43	5.182	6.933	8.685	10.436
加拿大/1800	0.72	1.561	2.522	3.483	4.756	6.028
加拿大/1900	0.188	0.195	0.214	0.232	0.302	0.371
中南美/1800	3.513	6.764	11.567	18.907	29.922	47.282
中南美/1900	1.21	2.799	4.977	7.176	10.313	13.449
日本	0.1	3.542	7.33	11.276	14.926	18.139
全球其他	6.912	13.613	21.965	32.12	42.809	52.777
合計	**17.328**	**37.826**	**66.003**	**98.678**	**136.569**	**179.642**

資料來源：工研院IEK，各公司網站，2000/6

TAIWAN CDMA手機相關廠商發展現況

廠商名稱	技術來源	發展現況	2000年產量推估	備註
明碁	QUALCOMM	CDMA/AMPS雙模手機即將出貨	約100萬隻	外銷到中南美洲ODM
致福	與韓M公司合作及技轉	已開始試產近期開始出貨	約20萬隻	外銷韓國OEM
大霸	PHILIPS	2001年開始量產	N/A	OEM
千煒	QUALCOMM	建廠中2001年開始出貨	N/A	QUALCOMM專業代工
金寶TELECOM	TELIAN/WIDE（QUALCOMM）	2000年開始量產	N/A	將會以泰寶（泰國廠）為生產基地ODM
仁寶	WACOM(購買韓廠以 建立能量)	已開始生產，預計10月開始出貨	60~70萬	ODM，銷往拉丁美洲
華碩	將為LGIC代工，另於美一家及於韓二家技轉中	2001年開始生產	N/A	將會以生產CDMA通訊模組為主
台達	N/A	建廠中	N/A	專業代工廠
廣達	與韓/美合作開發	開發中	N/A	專業代工廠
大眾	QUALCOMM	轉投資Gtran生產CDMA通訊模組已開始出貨	N/A	將會以WCDMA為發展目標

資料來源：工研院IEK，各公司網站，2000/7　中科院電子所整理

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CDMA晶片/技術供應商

廠商名稱	射頻（RF）IC	基頻／中頻（Baseband/IF)IC	備註
Philips/VLSI	SA95xx系列downconverter BGA20系列Transistor	CDMA+	提供CDMA protocol stack軟體
PraireComm	N/A	PCI 9501 cdmaOne PCI 2010 1X	由Qualcomm授權
Qualcomm	RFT3100 Transmit Processor IFR3000 Receive Process	MSM 3000系列 MSM 5000(支援cdma2000) CSM 5000基地台用晶片	提供CDMA TOTAL SOLUTION 包含PM power management IFR/IFT+RFR/RFT等IF IPROCESSOR 及PA3xx PA
DSP Communication/Intel		N/A 新款基頻將會於2Q00公開	原基頻IC由Qualcomm授權
RFMD			RF Front-END相關IC及Test Board
LSI		CBP	由Qualcomm授權 提供CDMA軟體
Tri-Quint	TQ3131、TQ3631 TQ5131、TQ5631		LAN(36系列) Down converter/mixer
Conexant	BAP (codec) RF25x (Tri-band CDMA RF Ics)		提供RF/IF(5 Chips design+PA)與Qualcomm基頻IC之Reference design
Motorola	In-house	In-house	
Ericesson	In-house	In-house	部份採用VLSI之晶片組
Nokia	In-house	In-house	
Analog Devices	N/A	AD6121 AD6122 IF amplifier/demodulator	
Sirus Communications		CDMA x	WCDMA基頻晶片
TI	TEL1101		CDMA CODEC
HP	MGA-72543		800/1.9DUAL BAND RF IC

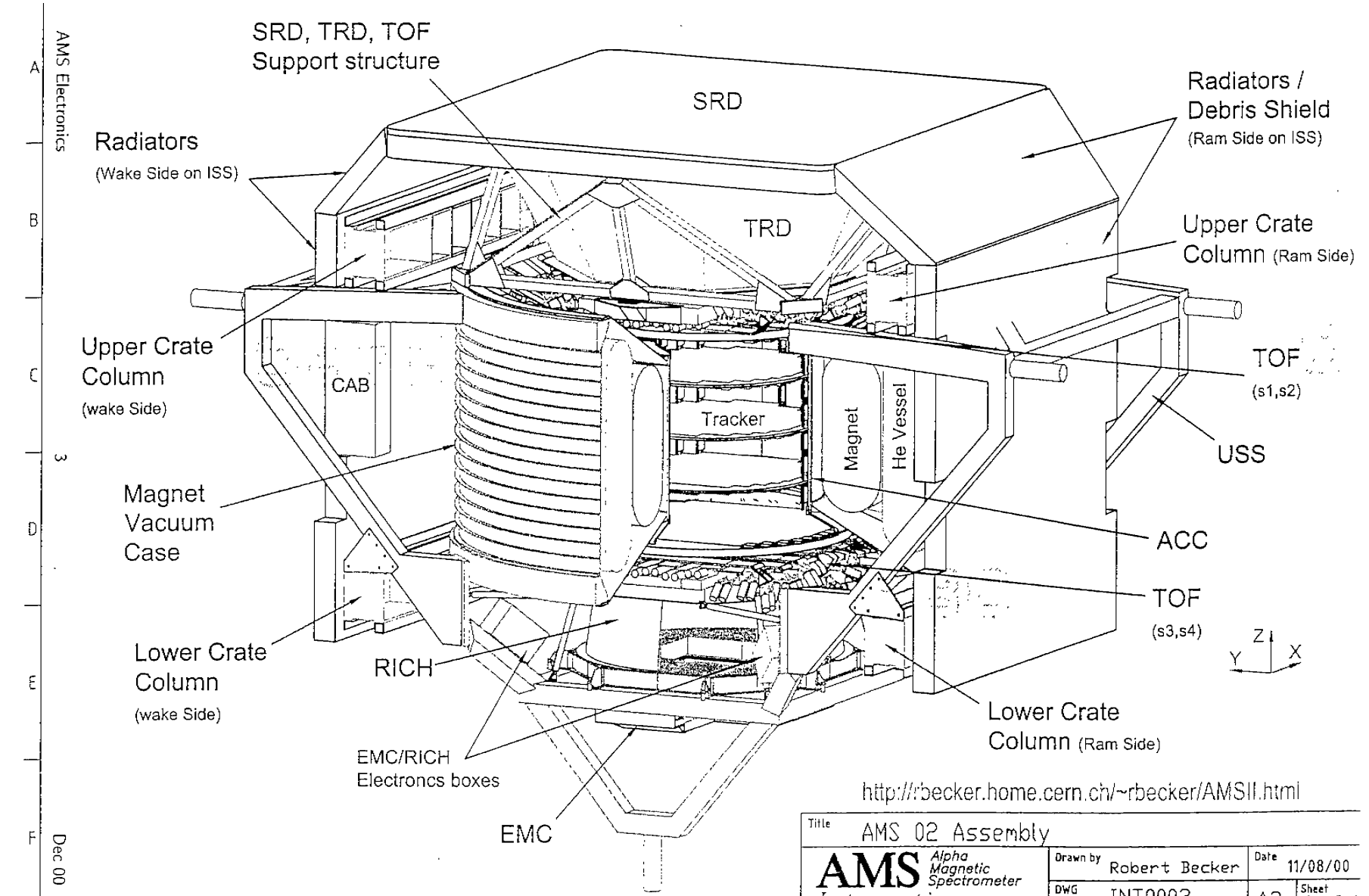
AMS Electronics

Dec 2000

Mike Capell/MIT

A few abbreviations:

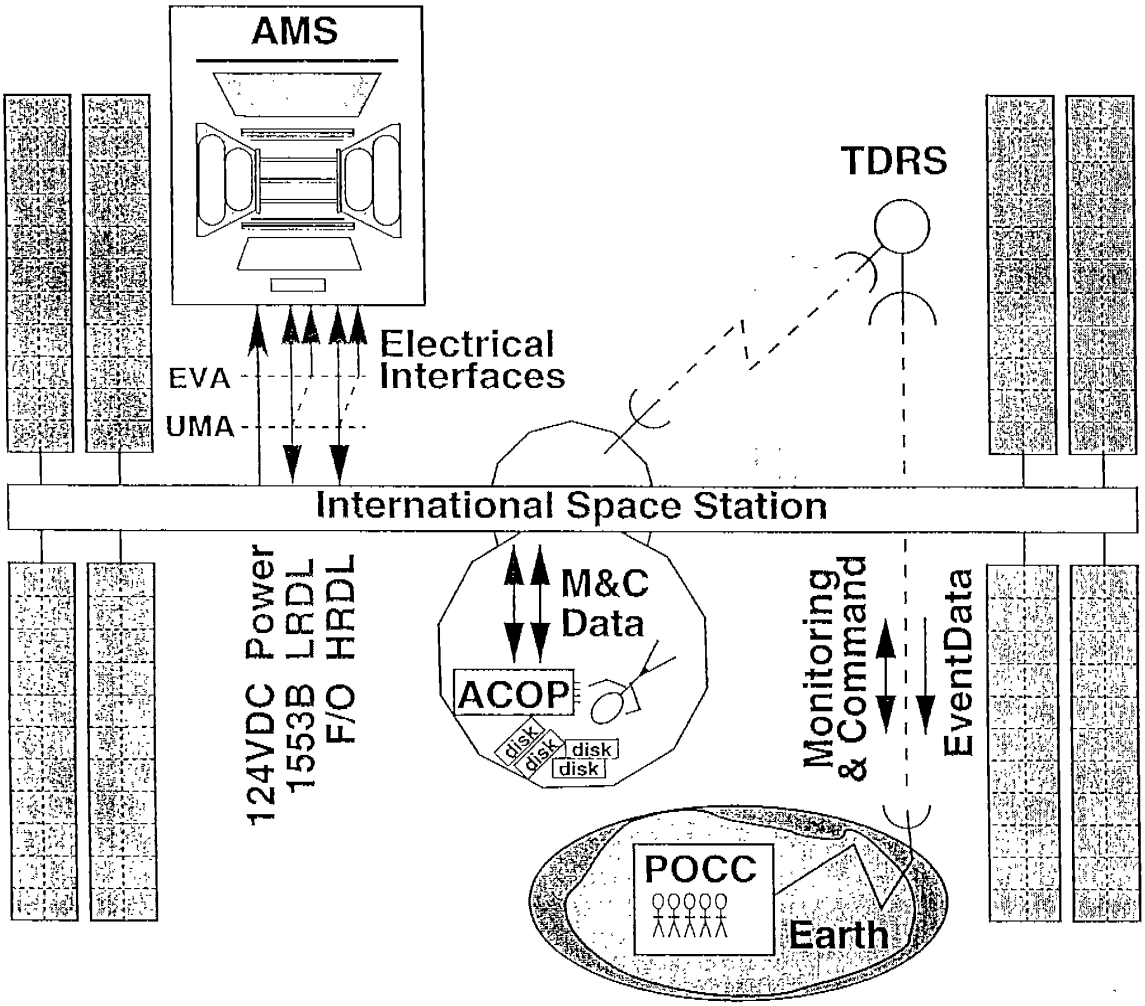
1H1C : "One hot, one cold"
1553B : Mil-Std-1553 B
ACC : AntiCoincidence (or Veto) Counters
ACOP : AMS Crew Operations Post
ADC : Analog to Digitial Converter (also A/D)
AMS : Alpha Magnetic Spectrometer
ASIC : Application Specific Integrated Circuit
B/H : Bulkhead
BP : Backplane
C : Initial for Cryomagnet related objects.
C & D : Command and Data
CAB : Cyromagnet Avionics Box
CAN : Controller Area Network
CCDB : Cryocooler Control & Drive Box
CCS : Cryomagnet Current Source
CCSC : Cryomag Controller and Signal Conditioner
CQMD : Cryomagnet Quench Monitor and Driver
CSP : Cyromagnet Self Protection unit
CVA : CryoValve Activator
DAC : Digitial to Analog Converter
DAQ : Data Acquisition
DSP : Digitial Signal Processor
E : Initial for EMC related objects.
ECAL : Electromagnetic Calorimeter (also EMC)
EDR : EMC Data Reduction
EFE : ECAL Front End
EHVC : EMC HV Controller
EHVG : ECAL HV Generator
EMC : Electromagnetic Calorimeter (a.k.a ECAL)
: also Electromagnetic Compatability
EMI : Electromagnetic Interference
EPC : ECAL Power Controller
EPD : EMC Power Distributor
F/O : Fiber Optic
FP : Front Panel
FPGA : Field Programmable Gate Array
Fmt. : Format
GA : Gate Array
HRDL : High Rate Data Link
HV : High Voltage
ISS : International Space Station
J : Initial for Trigger and DAQ related
J422 : RS422 Mulitplexer
JBP : J-crate backplane
JBU : JMDC BUffer
JET : ECAL Trigger
JFOM : Fiber optic Multiplexer
JIM : JMDC Interface Module
JINx : DAQ Intermediate node, type "x"
JMDC : Master DAQ Computer
JMTT : Master Trigger/Timing
JPC : Trigger & DAQ (J-crate) Power Controller
JPD : DAQ & Trigger Power Distributer
JSBC : JMDC Single Board Computer
JTRG : Main Trigger
LAB : Laser Alignment Box
LRDL : Low Rate Data Link
M : Initial for Monitoring & Control stuff
M&C : Monitor and Control
MCB : Monitor & Control Box
MCC : Monitor & Control Computer
MCSx : Monitor & Control Sensor electronics, type "x"
MEM : Memory
OTL : Out to lunch
P : Initial for Power related objects.
PAS : Payload Attachment System
PCA : Printed Circuit Assembly
PCB : Printed Circuit Board
PDB : Power Distribution Box
PMT : Photo Multiplier Tubes
POCC : (our) Payload Operations and Control Center
R : Initial for RICH related objects.
RDR : RICH Data Reduction
RFE : RICH Front-End
RHVC : RICH HV Controller
RHVG : RICH HV Generator
RICH : Ring Imaging CHerenkov detector
RPC : RICH Power Controller
RPD : RICH Power Distributor
RT : 1553B Remote Terminal
S : Initial for Scintillator related objects.
SBP : Scintillator BackPlane (not foreseen).
SDR : Scintillator Data Reduction
SFEA : Scintillator Front End: ACC
SFED : Scintillator Front End: Dynode
SFET : Scintillator Front End: ToF
SHVC : Scintillator HV Controller
SHVS : Scintillator HV Supply
SPC : Scintillator Power Controller
SPF : Single Point Failure
SPD : Scintillator Power Distributor
STS : Space Transport System (the Shuttle)
SW : Side Wall
T : Initial for tracker related objects.
T/T : Trigger and Timing
TBP : Tracker BackPlane
TBS : Tracker Bias Supply
TDC : Time to Digitial Converter
TDR : Tracker Data Reduction
TDRS : Tracking and Data Relay Satellite
TFEx : Tracker Front End, type "x"
TPC : Tracker Power Controller
TPD : Tracker Power Distributer
TPSFE : Tracker Power Supply, Front End
TRD : Transition Radiation Detector (initial "U")
ToF : Tome of Flight
Tot. : Total
U : Initial for TRD related objects.
UBP : TRD BackPlane
UDR : TRD Data Reduction
UFE : TRD Front End
UGBC : TRD Gas Box "C" (Control)
UGBS : TRD Gas Box "S" (Supply)
UHVC : TRD HV Controller
UHVG : TRD HV Generator
UHVS : TRD HV Supply
UMA : Umbilical Mechanical Attachment
UPC : TRD Power Controller
UPD : TRD Power Distributer
UPSFE : TRD Power Supply, Front End
USCM : Universal Slow Control Module
ZFT : Zero Fault Tolerant



http://rbecker.home.cern.ch/~rbecker/AMSII.html

Title: AMS 02 Assembly			
AMS Alpha Magnetic Spectrometer Integration	Drawn by: Robert Becker	Date: 11/08/00	
	DWG: INT0003	A3	Sheet: 1 of 1

AMS::ISS Interfaces



Power, Low Rate and High Rate interfaces:

- For ISS: PAS (mechanical) contains UMA (connector).
- For STS: PEDS connected to shuttle electronics.
- On Pad: PEDS connected via T0 to ... to AMS-GSE.
- Before: Direct connections to AMS-GSE.

AMS DAQ Scale:

"Channels"	*AMS 01*	AMS 02	type
Si Tracker	*65,536*	196,608	Strips; Ampltude
ToF + ACC	*480*	384	PMT; Time, Amp. & Trigger
Cerenkov	*84*	33,792	PMT pixel; Amp.
TRD	-	5,248	Wire; Amplitude
ECal	-	2,592	PMT Pixel; Amp. & Trigger
	-		
DAQ Links			
Total	*238*	? 686	
Active	*99*	? 279	

Raw data rate:

5 Mbit $\otimes$ 200-2000 Hz $=$ 1 – 10 Gbit/sec.

(1000 day mission total $>$ 10^{17} bits)

Data reduction, filtering:

12 Kbit $\otimes$ 160 Hz avg. $=$ 2 Mbit/sec,

or 1GByte/hour

24

Crate, Card and Box Counts

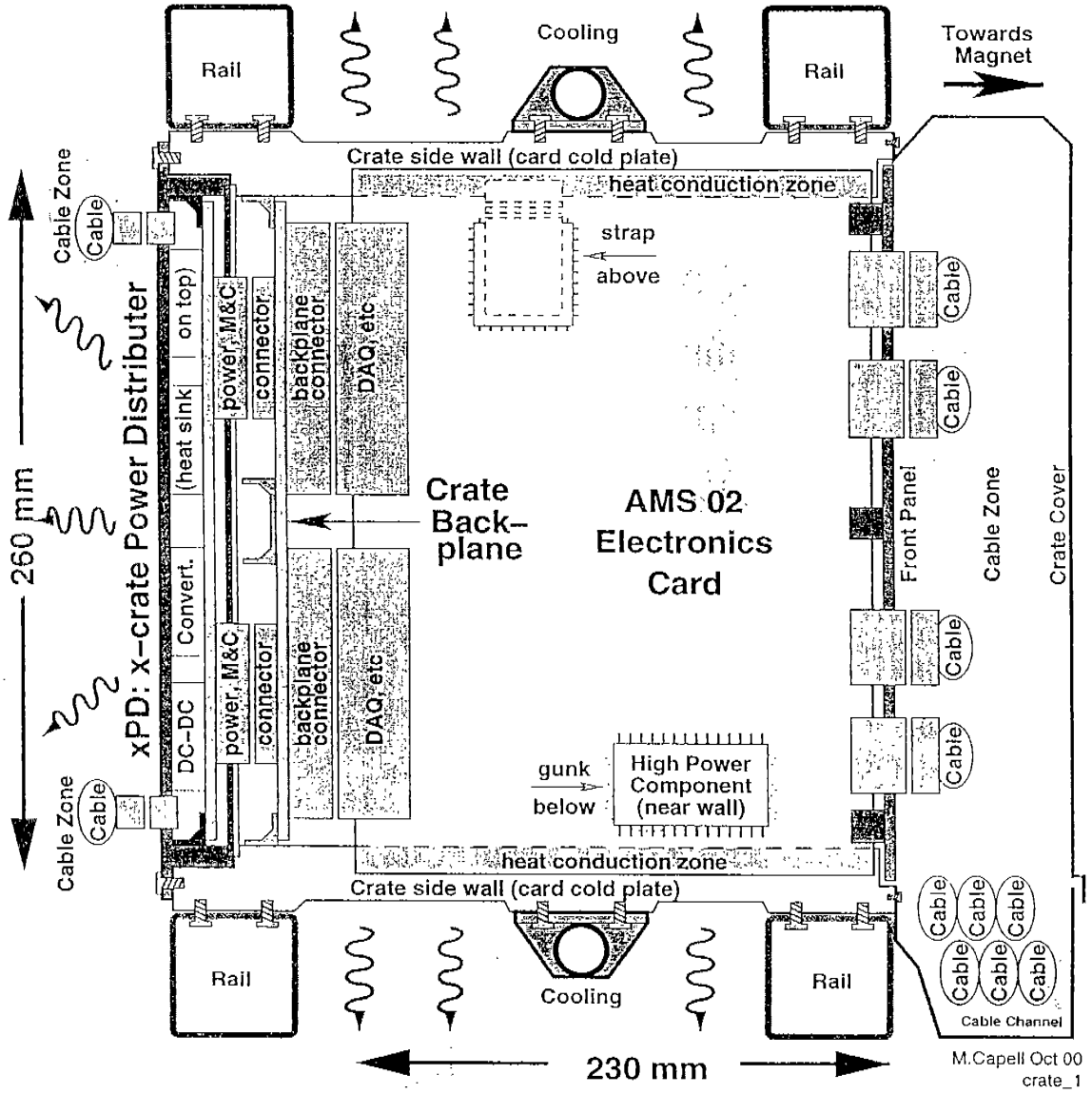
Crates:

Qty	Name	Cards	Function	Location
✓8	T-crate	21	Tracker	2/rack
✓2	U-crate	15	TRD	1/upper racks
4	S-crate	9	ToF+ACC	1/rack
4	R-crate	? 8	RICH	lower strut
? 4	E-crate	? 8	ECal	lower strut
✓1	J-crate	22	DAQ & Trigger	lower ram rack
2	CCDB	3	Cyrocoolers	1/upper racks
1	PDB	12	power	lower wake rack
4	MCB	5	M & C, thermal	1/rack
1	LAB	5	alignment	tbd.
		∼ 360	cards plus power supplies.	
∼ 31	crates of 10 types (AMS 01: 22 of 6 types)			

Other boxes:

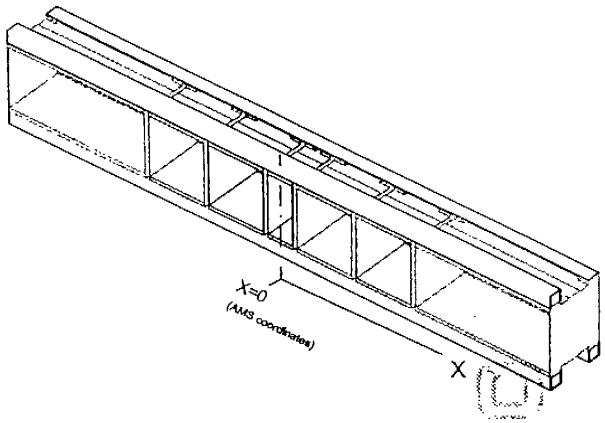
Qty	Name	Function	Location
1	UGBS	TRD gas	wake port
1	UGBC	TRD gas	wake port
1	UGE	TRD gas elec.	wake port.
1	CAB	Magnet	wake starb.
1	CVA	Magnet valves	wake center

AMS 02 Crate Thermo/Mechanical Sketch

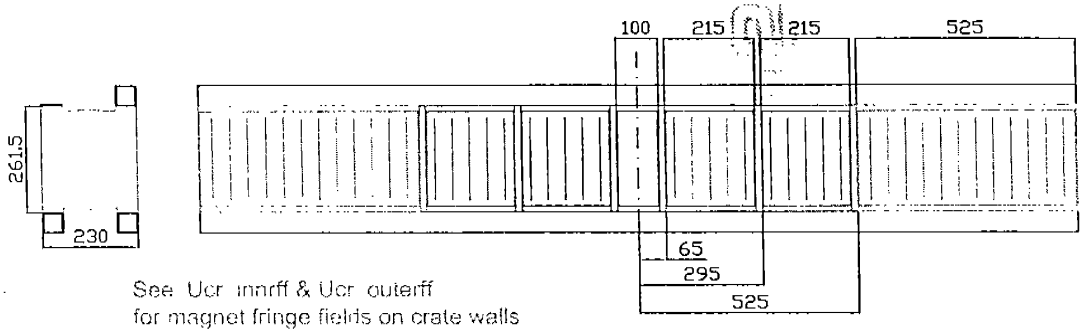


Crate design started by Carlo Gavazzi Space, Milano.

→ STD VME cards

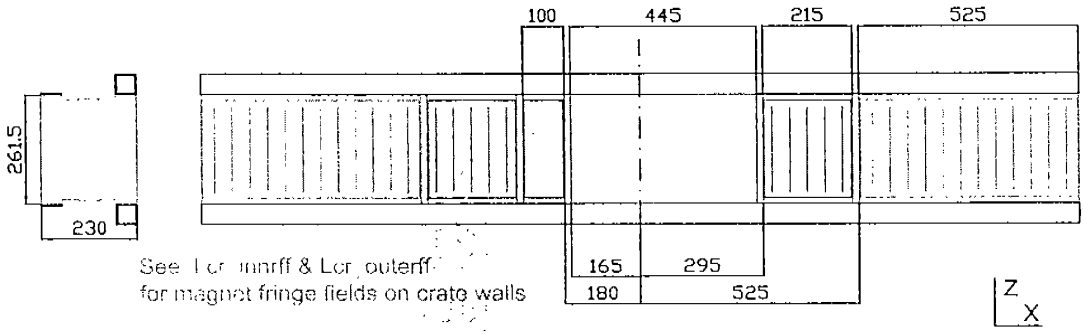


Upper Crate Column



See Ucr innrff & Ucr outerff
for magnet fringe fields on crate walls

Lower Crate Column



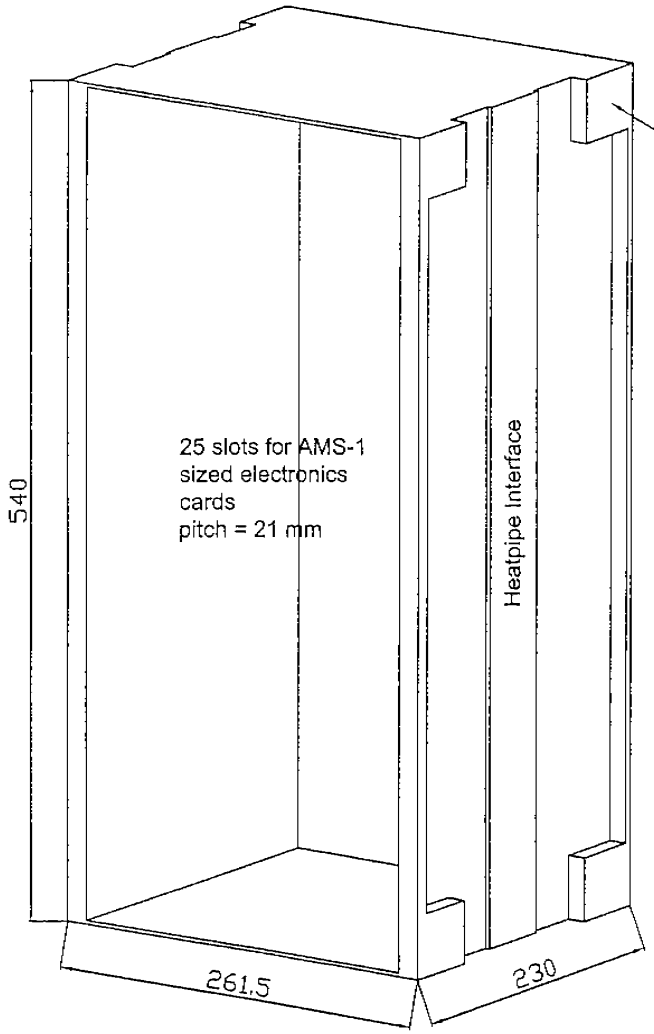
See Lcr innrff & Lcr outerff
for magnet fringe fields on crate walls

For this Crate rack design the thickness (261.5 mm) and back vertical wall position (in Y) are fixed. if needed crates can be made deeper (230mm+) such that they prodrude past the box beam structure towards AMS. Crate length (X) can also be negociated.

Checked by	Approved by	Auth	Am. Projection
Crate Rack Assembly	Preliminary		Scale
AMS Alpha Magnetic Spectrometer Integration MIT	Drawn by Robert Becker		Date 28/04/00 Dec 00
	DWG INTcr05	A3	Sheet 1 of 1

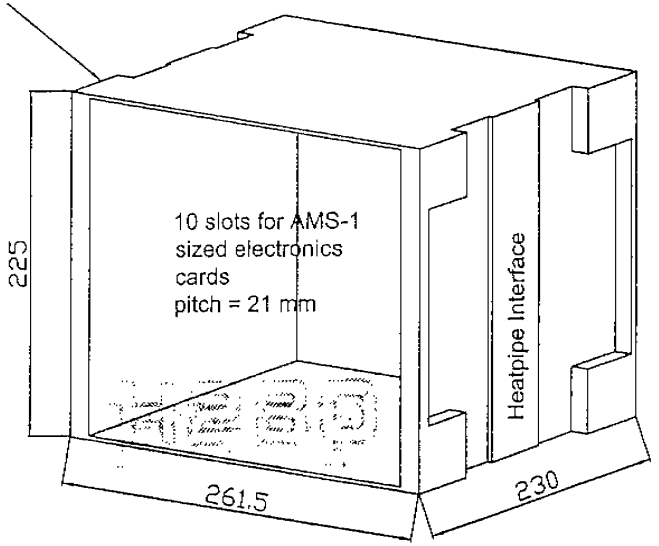
AMS Electronics

Large Crate



Rack interface
(4 corners)
(1 or 2 shearbolts)

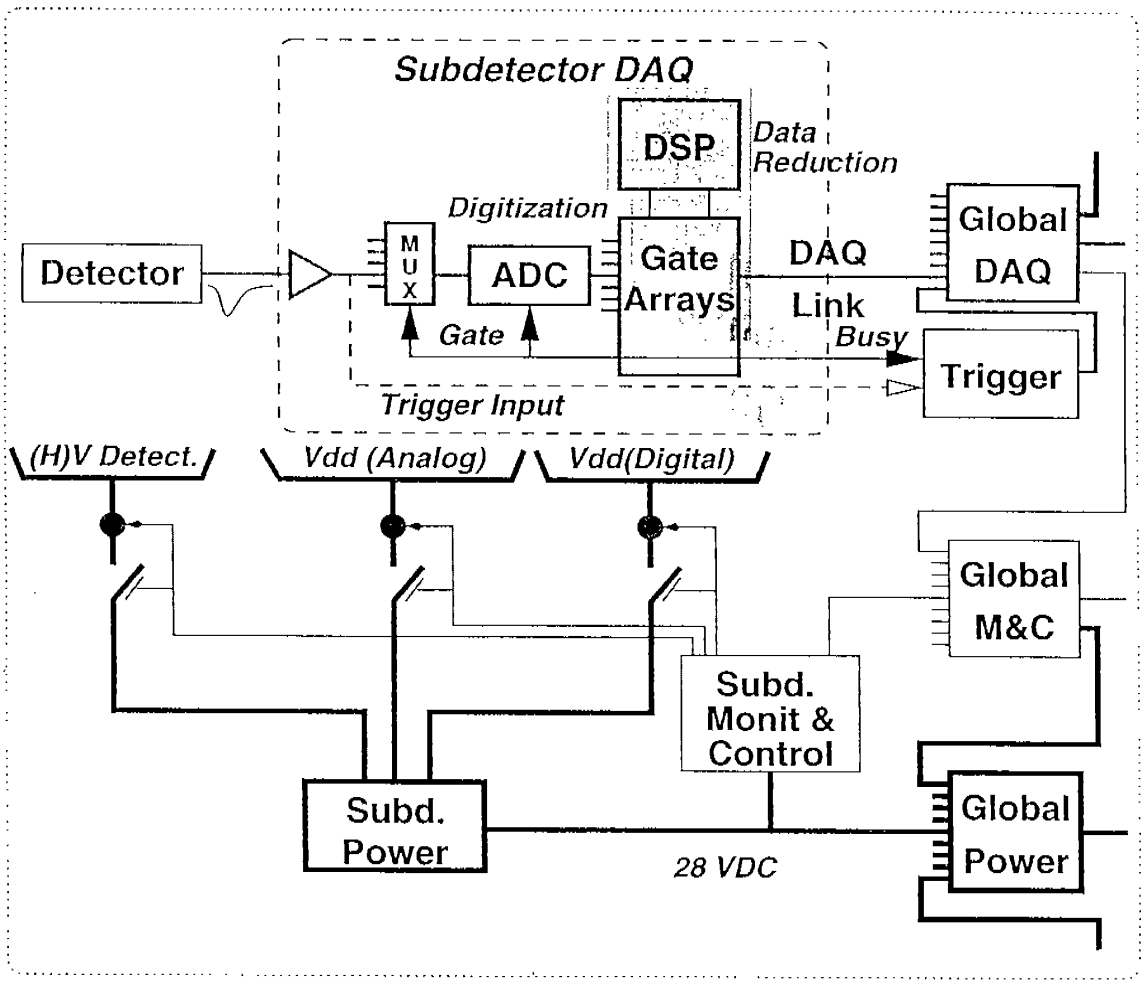
Small Crate



Checked by	Approved by	Auth	Am. Projection
Preliminary Electronics Crate Dimensions			Scale
AMS Alpha Magnetic Spectrometer Integration MIT	Drawn by Robert Becker		Date 26/04/00
	DWG INTcr03	A3	Sheet 1 of 1

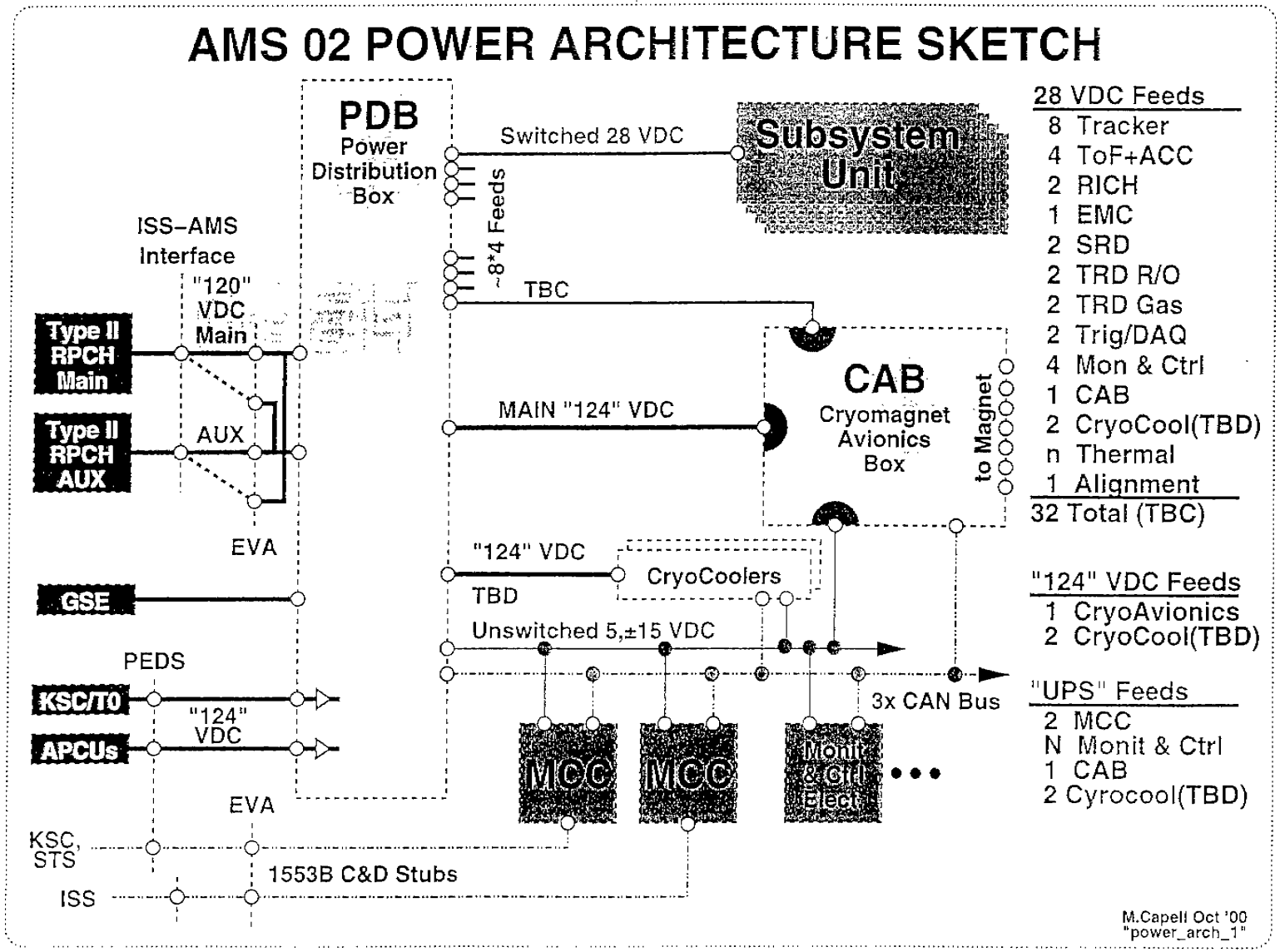
Dec 00

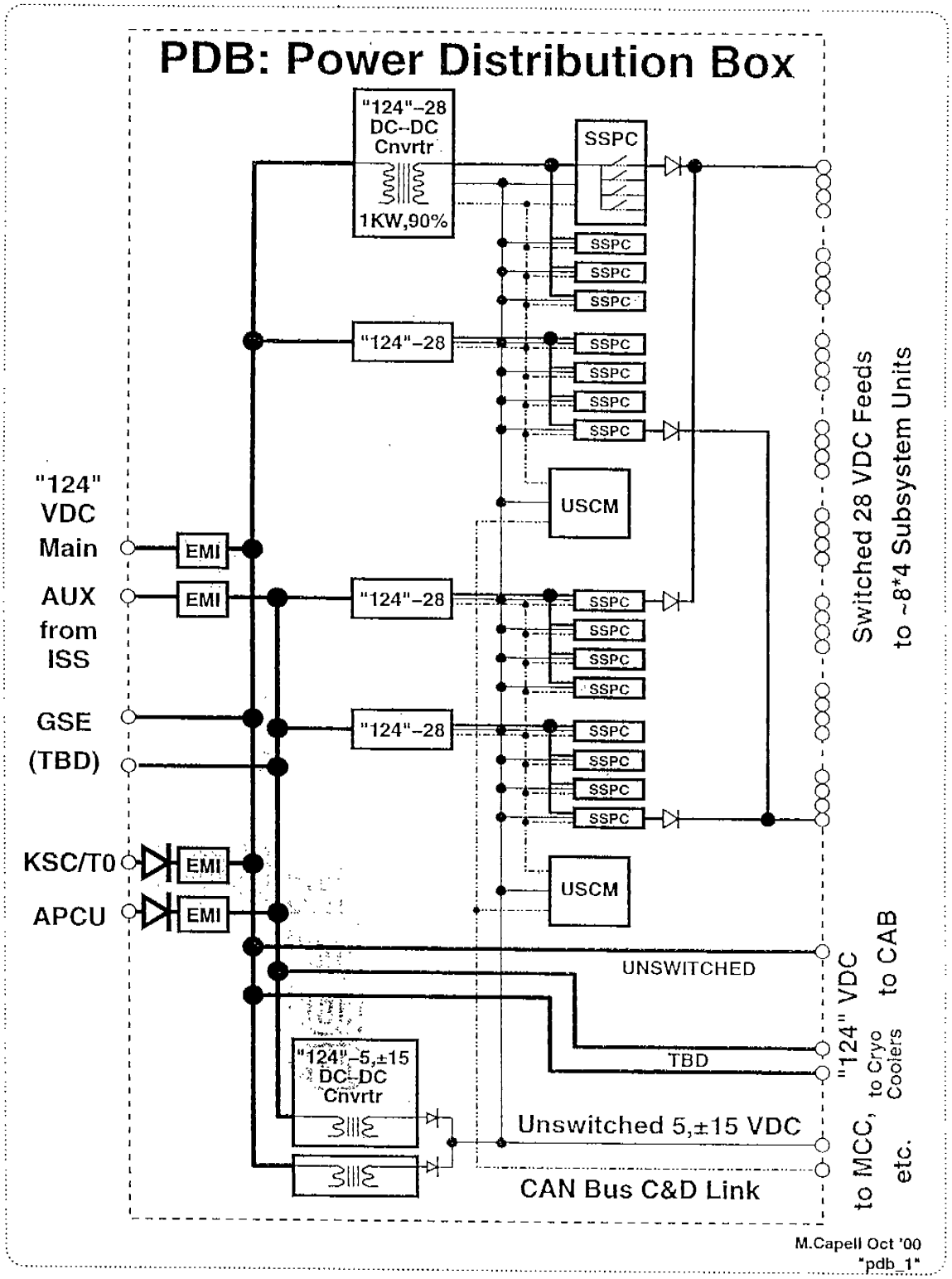
Typical Subdetector Electronics Scheme:



- Subdetector specific parts:
  Digitization, Timing signals (Gate, Busy), Trigger Inputs, HV and analog power supplies.
- Subdetector common parts:
  DSP to GA interface, DAQ Links,
  Digital power supplies and power supply control.
  Much in common with upper DAQ levels (JIN) boards.

CD DL


AMS 02 POWER ARCHITECTURE SKETCH
PDB
Power Distribution Box
Switched 28 VDC
Subsystem Unit
~8*4 Feeds
TBC
ISS–AMS Interface
"120" VDC Main
Type II RPCH Main
Type II RPCH AUX
AUX
EVA
MAIN "124" VDC
CAB
Cryomagnet Avionics Box
to Magnet
"124" VDC
TBD
CryoCoolers
Unswitched 5,±15 VDC
GSE
PEDS
KSC/TO
APCUs
"124" VDC
3x CAN Bus
MCC
MCC
Monit & Ctrl Elect
EVA
KSC, STS
1553B C&D Stubs
ISS
28 VDC Feeds
8 Tracker
4 ToF+ACC
2 RICH
1 EMC
2 SRD
2 TRD R/O
2 TRD Gas
2 Trig/DAQ
4 Mon & Ctrl
1 CAB
2 CryoCool(TBD)
n Thermal
1 Alignment
32 Total (TBC)
"124" VDC Feeds
1 CryoAvionics
2 CryoCool(TBD)
"UPS" Feeds
2 MCC
N Monit & Ctrl
1 CAB
2 Cyrocool(TBD)
M.Capell Oct '00
"power_arch_1"


PDB: Power Distribution Box
"124"-28 DC-DC Cnvrtr
1KW,90%
SSPC
"124" VDC Main
AUX from ISS
GSE (TBD)
KSC/T0
APCU
EMI
"124"-28
USCM
Switched 28 VDC Feeds to ~8*4 Subsystem Units
UNSWITCHED
TBD
"124" VDC to CAB
to Cryo Coolers etc.
to MCC,
"124"-5,±15 DC-DC Cnvrtr
Unswitched 5,±15 VDC
CAN Bus C&D Link
M.Capell Oct '00
"pdb_1"

Power Architecture

- 124 VDC converted to 28 VDC in PDB.
- Each crate or box receives one (or two) 28 VDC feeds.
- DC–DC converters to useful (3.3, 5, 12, 2500, ...) VDC.
- Common specifications for these converters agreed.
- CAEN is designing custom converters for AMS 02:
  Pro: high-efficiency, low-noise, flexible.
  Con: flight experience, discreet.
- Also using common approach to power monitoring and control based on USCM card from Aachen.

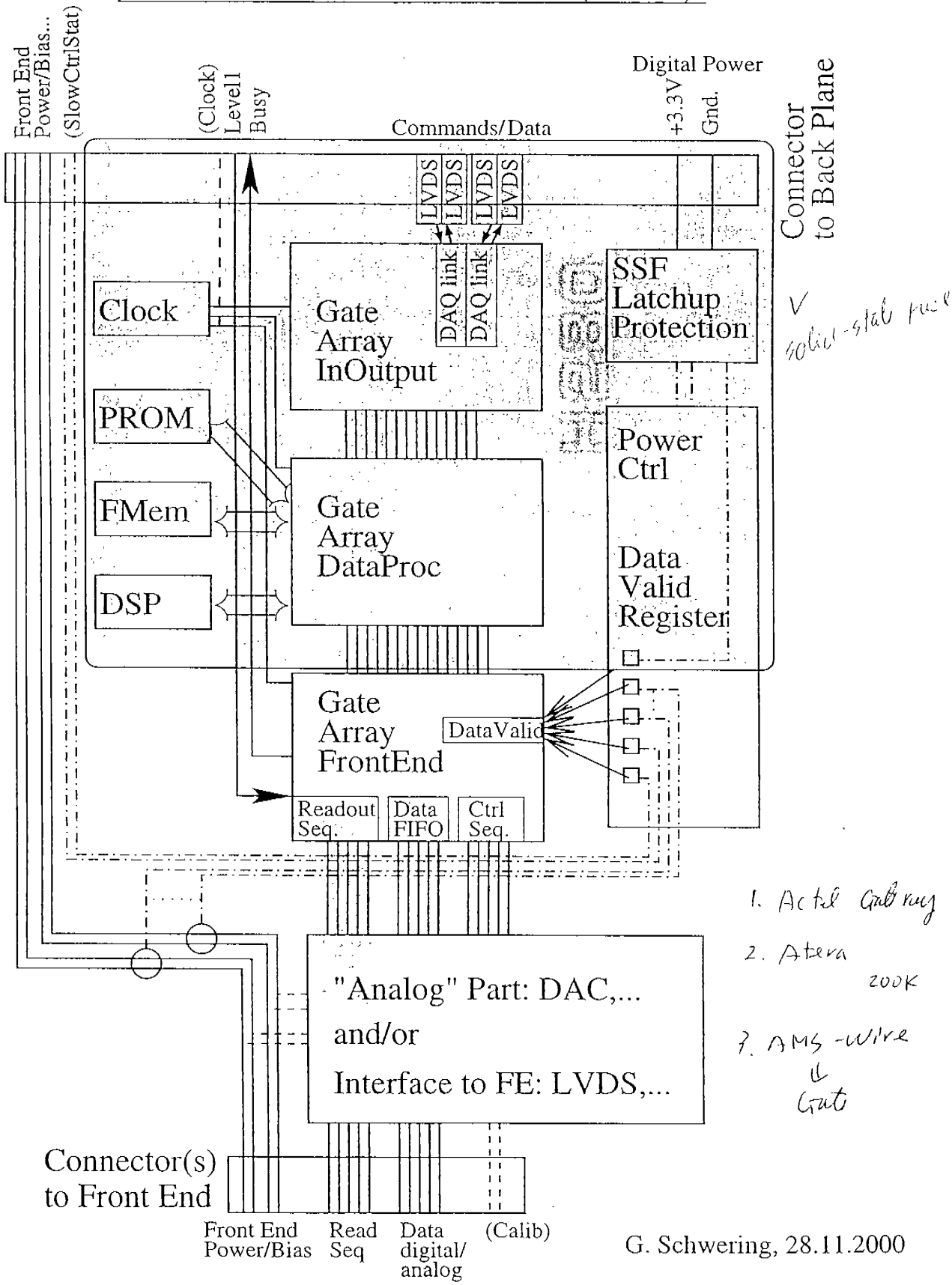
ISS can provide only 2000 Watts:

Power is tight.

We also need thermal management to get rid of the waste heat from every watt we consume. (loops, pumps, radiators).

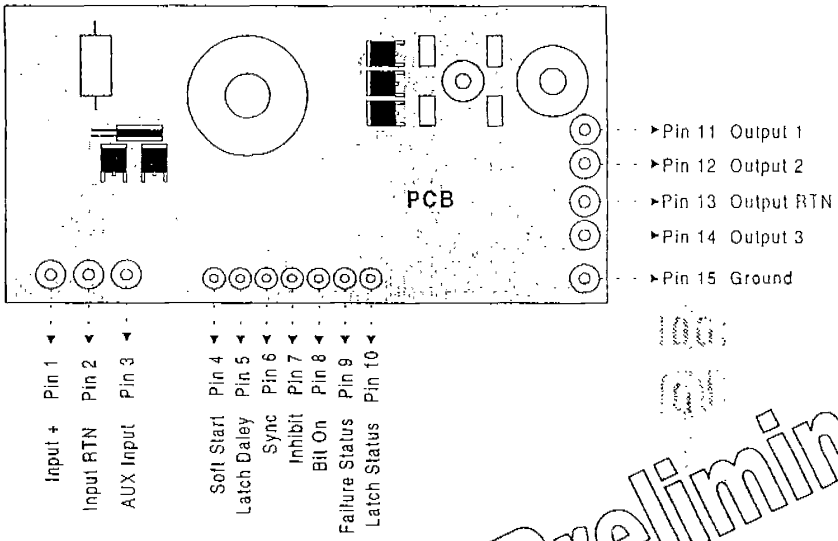
Revised CRATE WALL thermal specs:
Storage: -40 to $+70$ C.
Operation: -20 to $+50$ C.

Data Reduction Unit (xDR)



G. Schwering, 28.11.2000

4.3 S90XX PROTOTYPE – PRELIMINARY DATA SHEET



DC/DC S90XX prototype layout

Electrical Specification

Type	V Input	Output 1		Output 2		Output 3	
	[V]	Vout [V]	Iout max [A]	Vout [V]	Iout max [A]	Vout [V]	Iout max [A]
S9021	28 ±1.5	+5.6	0.9	+2.6	1.2	-2.6	2.4
S9022	28 ±1.5	+5.6	1.1	-5.6	1.1	==	==
S9023	28 ±1.5	+3.6	6.9	==	==	==	==
S9024	28 ±1.5	+5.3	4.7	==	==	==	==
S9025	28 ±1.5	+120.0	0.01	+6.0	0.2	-6.0	0.2
S9026	28 ±1.5	+12.0 (TBC) (1)	TBD (1)	TBD (2)	TBD	==	==
S9027	28 ±1.5	+3.6	TBD (3)	-2.6	TBD (3)	==	==

NOTE

(1) To be defined according to CAEN custom solution for the control parts supply voltage specification.

(2) To be defined if will be added a +5.xV for the CAN bus channel in the xPC board based on USCM board.

(3) It is fixed the maximum output power to 10W, to be defined according, to RICH Front End chip request, the unbalancing between the two channels.

→ System Loading

AMS-2 JSBC and JBU Development Preliminary Design Review (PDR)

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28-NOV-2000

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附件六

Agenda

- Requirement
- Design Goals
- Radiation Harden Assurance
- JSBC and JBU Design Specification
- Design Approach
- Risk
- Schedule and Milestone
- Conclusion

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Requirement

- Functional requirement
- Input/Output requirement
  - Power requirement(TBD)
  - Data bus requirement
  - Communication requirement
- Physical requirement(TBD)
  - Size,shape,connector....
- Reliability requirement
- Environmental requirement

Functional Requirement

- Collating event data from the intermediate DAQ
- Applying the level-3 filter algorithm
- Collecting a copy of the monitoring data (for MCC ?)
- Blocking, formatting and buffering both the event and monitoring data for the HRDL

From Mike Capell's Presentation Material

Environment Requirement

- Static Loads 40+10+10g
- Random Vibration to 6.3g (rms)
- Vacuum
  - Heat dissipation by conduction and radiation
- Thermal range
  - Storage : -40 ° to 80 ° C.
  - Operation : -30 ° to +60 ° C.
- Radiation Dose ~Kilorad/year
- Heavy ion single event effects
- Stray magnetic field up to a few hundred Gauss
- EMC
- Lifetime : 1year test, 3+ years no access

From Mike Capell's Presentation Material

Design Goals

- High performance CPU to manage event data and max. data throughput
- Large buffer memory to store the data
- Low power consumption
- Different type communication channel and data routing scheme
- Operate adequately in the radiation environment.
- 4 redundant Main DAQ computer(JMDC)
  - PowerPC750 single board computer
  - 2G bytes memory buffer
  - Interface module (CAN, AMS-wire, HRDL, RS-422)
- Trade-off
  - Availability, power, volume, performance and cost of radiation-hardened devices
- SEE mitigation
  - Hardware, software, device tolerance requirements

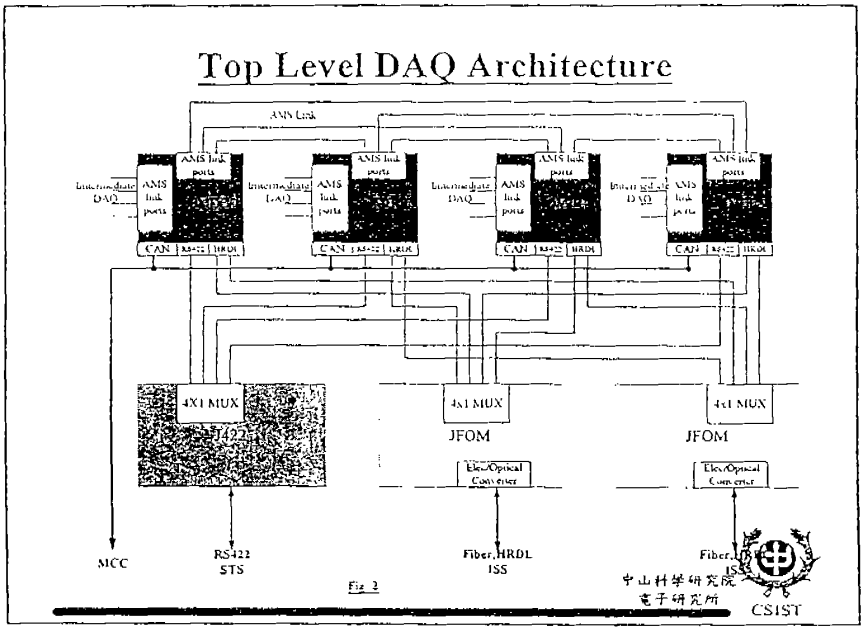
Top Level DAQ Architecture
AMS Link
AMS link ports
Intermediate DAQ
AMS link ports
CAN
RS422
HRDL
4X1 MUX
4x1 MUX
JFOM
4x1 MUX
JFOM
Elec/Optical Converter
Elec/Optical Converter
MCC
RS422
STS
Fiber HRDL
ISS
Fiber
ISS
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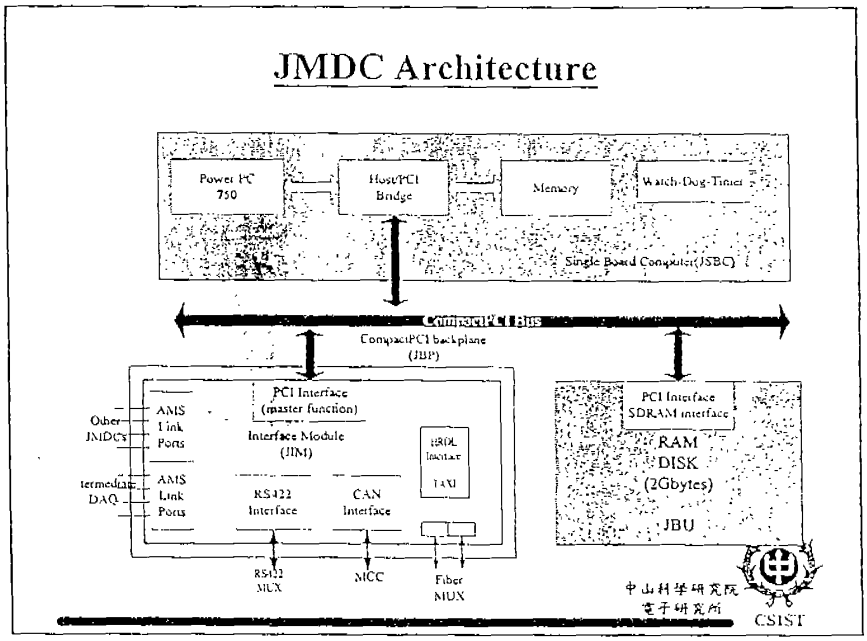
Fig. 3


JMDC Architecture
Power PC
750
Host/PCI
Bridge
Memory
Watch-Dog-Timer
Single Board Computer(JSBC)
CompactPCI Bus
CompactPCI backplane
(JBP)
PCI Interface
(master function)
Other
JMDCs
AMS
Link
Ports
Interface Module
(JIM)
HRDL
Interface
FIFO
Intermediate
DAQ
AMS
Link
Ports
RS422
Interface
CAN
Interface
PCI Interface
SDRAM interface
RAM
DISK
(2Gbytes)
JBU
RS422
MUX
MCC
Fiber
MUX
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Design Overview

- Concept development
  - Survey of space qualified components
  - Investigate radiation effect mitigation design methods
  - Tradeoff study different approaches
- Prototyping Hardware
  - Provide prototype board design specification
  - PLD and Board Implementation
  - Test code generation
- Flight Version Hardware
  - Fix hardware problems discovered in prototype board
  - Find solutions that made use of available parts
- Integration Test

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Evaluation and Integration

- Operation Test
  - Perform to verify the operational readiness and localize malfunction
- Qualification and Reliability Test
  - Test in CSIST
  - Test item: TBD
  - Supplement test equipment: TBD
  - Test procedure: TBD
  - Test specification: TBD
- Integration with detectors
  - Test in ETH
  - Test in KSC

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Radiation Harden Assurance

- HA Program management
- HA Design support
- HA Test and analysis
- HA demonstration and inspection
- Configuration management
- Parts and materials control
- Quality management
- Production controls
- HA training

MIL-HDBK-817

System Development Radiation Hardness Assurance

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Parts Control

- Strategy for pre-selecting components and qualifying batches
- Procurement strategy
- Standard test methods
  - Total ionizing dose, single event effects
- List of the components used in this project
  - Build the electronics components data base
  - Collect available data
- Setup irradiation facilities
- Define Derating Rules

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SEE Mitigation Technique-Control

- Watchdog timer to monitor operation
  - Implemented in hardware or software
  - Active or passive
  - Multi-level, subsystem to subsystem, board to board, device to device ..
- Redundancy hardware
  - Provide means of recovery from a SEE on a system level
  - Operating two identical circuits with synchronized clock
  - Voting to choose the output that at least two agree
- Redundancy command structure
  - Two commands trigger an event with different data or address
- Current limiting circuit
- Recycle power

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SEE Mitigation Technique-Memory

- Parity check
  - Single bit error detect
- CRC (cyclic redundancy check) code
  - Detects if any errors occurred in a given data structure
- Hamming code
  - Single bit correct, double bit detect
- Reed-Solomon code
  - Correct consecutive and multiple bytes in error
- Convolution encoding
  - Correct isolated burst noise in a communication stream
- System level protocol
  - Retransmission data

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JSBC and JBU Design Specification

- JSBC Prototype Board Hardware Design Specification
  Initial issue:OCT-12-2000
  Document No. CSIST-AMS-MDC-001
- JBU Prototype Board Hardware Design Specification
  Initial issue:OCT-13-2000
  Document No. CSIST-AMS-MDC-001

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JSBC Prototype Feature(I)

- CPU (Central Processing Unit)
  - PowerPC750
  - 6 execution units
  - 32K bytes Instruction & Data non-blocking L1 caches
  - Dual Memory Management Units (MMU)
  - On-chip debug support (COP and JTAG)
  - Advanced power management
  - 64-bit data 32-bits address
  - Processing performance at 488MIPS@266 Mhz, 733MIPS@400 Mhz
- Memory
  - Boot PROM: 128K bytes, 8-bits wide
  - Flash EPROM: 16M bytes, 16-bits wide
  - SDRAM: 144 Pin SO-DIMM SDRAM socket supports up to 256M bytes, data bus width 72-bits with 64 bits data and 8 bits ECC

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19/12 Video Conference

JSBC Prototype Feature(II)

- 12 external interrupts, individually maskable
- PCI 2.1, 32-bits, 33Mhz, with 5 bus arbiter (REQ/GNT signal)
- Watchdog timer and supervisory circuit
- Power-on-reset, external reset
- Timer to monitor the CPU operation
- Power supply monitor
- On-board Peripheral
  - Serial I/O: Two 2-wire UART (16500 compatible)
  - General purpose timer: 32-bits time base, 5 capture event timers and 5 compare timers
  - IIC interface : two independent IIC interface
  - Control register: Control/status registers, Watchdog restart/read, enable/disable register
- CompactPCI system slot, PICMG 2.0 compliant
- Form Factor : 9.19 inches by 6.3 inches CompactPCI 6U board size with conduction cooled

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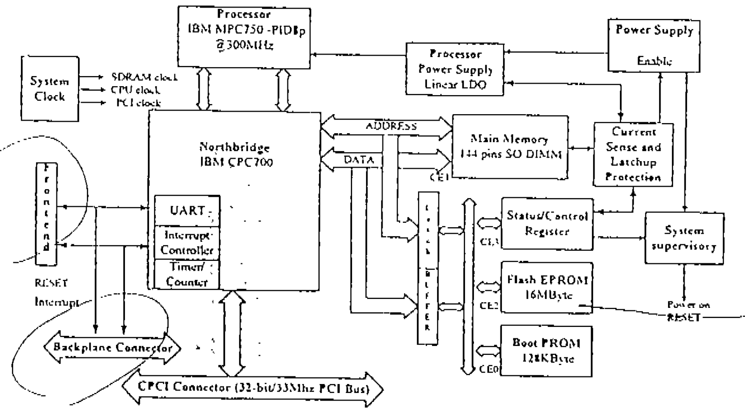
JTAG

Power on

AMS wire boot cmd"

Select small AMS model, HRDL boot CMD. /RS422 [Button] → prototype & latch w/ power sensing WATCHDOG

JSBC Prototype Block Diagram



JSBC(MDC Single Board Computer)Block Diagram

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32MB?

Power on
Reset
Boot
Boot from BOOT PROM
Wait for CMD from
a) CAN
b) AMS wire (another MDC)
c) HRDL/RS422
This CMD will be
a) boot from EPROM (default) b) boot from follows c) write what follows to EPROM

1. individual JTAG (not daisychain) for JSBC

JBU Prototype Feature

- Memory
  - SDRAM: Available capacity range from 1G bytes to 2G bytes(dependent on SDRAM technology in the commercial environment thus ensuring future availability of higher capacity.)
  - 2 individual memory section architecture with latch-up protection circuit, can be powered on and off separately
- SDRAM control function
  - Support auto pre-charge mode and burst mode
  - Provide four commands: Mode register write, burst write, burst read, refresh
  - Automatic refresh
  - Low clock skew between FPGA and SDRAM
- PCI 2.1 compliant, 32-bits/33Mhz target function
- CompactPCI peripheral slot, PICMG 2.0 compliant
- Form Factor : 9.19 inches by 6.3 inches CompactPCI 6U board size with conduction cooled

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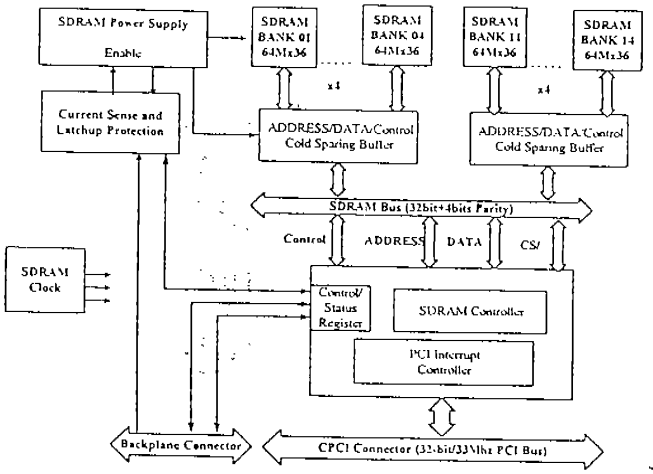
JBU Prototype Block Diagram



JBU(Memory Buffer)Block Diagram

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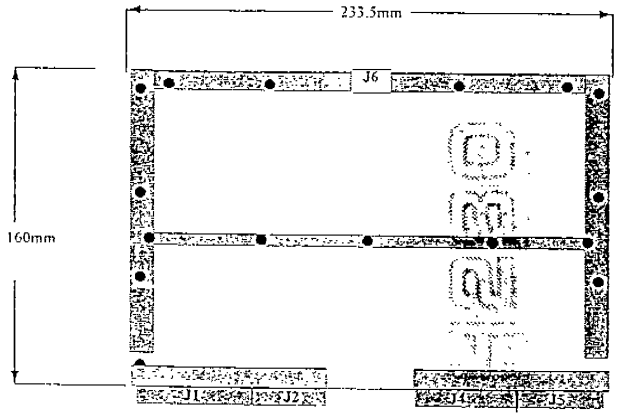
Physical Board Dimension



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Design Approach

- Study circuit of evaluation board
- Adopt the example circuit for design
- FPGA logic design and simulation
- PCB schematics
- Boot code and test code generation
- PCB placement and routing
- PCB manufacture and assembly
- Debugging
- Functional test and verification

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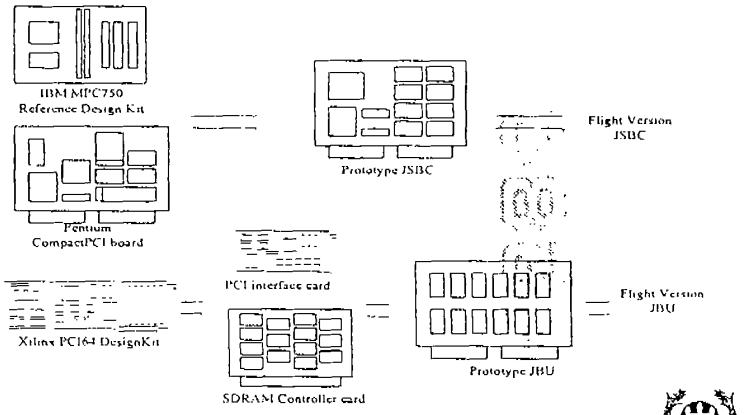
PLD and Board Implementation



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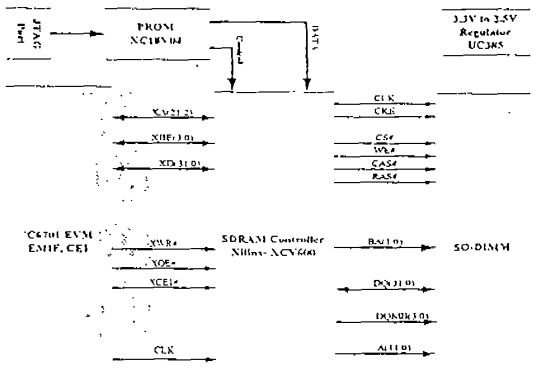
SDRAM Controller Evaluation Board



SDRAM 測試面路版方塊圖

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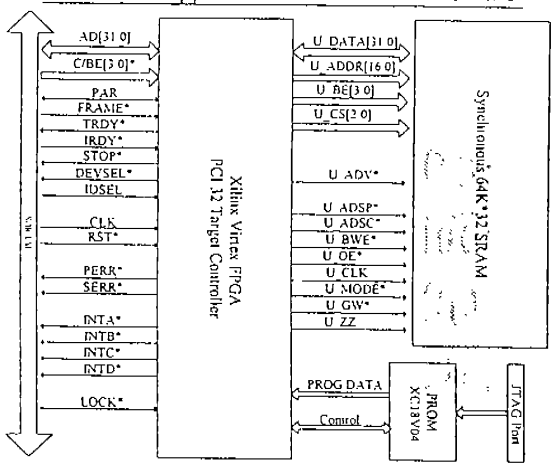
PCI Target Evaluation Board



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Radiation Effect Consideration

- Radiation harden component
  - Expansive and lead time uncertainly
- Radiation-shielding Conformal Coating
  - SEI RAD-COAT , for total ion dose
- Shielding
- ACTEL vs. Xilinx
- EEPROM vs. PROM
- EDAC vs.Parity check

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Risk

- The primary risk is the radiation qualification problem for components which are needed to provide the performance at low power.
- The judgment and examination of CPU performance to manage the complexity of data channels.
- SEE mitigation method depends on many factors which must be considered at the system and project level

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Schedule Milestones

- OCT,2000 first issue JSBC design specification
- OCT,2000 first issue JBU design specification
- Jan,2001 JSBC prototype board circuit design ✓
- Mar,2001 JBU prototype board design circuit design ✓
- Jun,2001 JSBC prototype board delivery
- Jul,2001 JBU prototype board delivery
- Time TBD JSBC flight version specification confirm
- Time TBD JBU flight version specification confirm
- Time TBD JSBC flight version board delivery
- Time TBD JBU flight version board delivery

Integration Test ?

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Conclusion

- Need more sample methods and design techniques to reduce radiation effect impact
- Availability of space qualified components
- Firm up the requirements, changes allowed with little impact to design
- Limit R&D manpower, schedule contingent on the loading of other projects

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- Design examples
  - Component
- 人力

JSBC Block Diagram